HP 4291B RF Impedance/Material Analyzer

SERVICE MANUAL

SERIAL NUMBERS

This manual applies directly to instruments with serial number prefix JP1KE, or firmware revision 01.00.
For additional important information about serial numbers, read "ANALYZERS COVERED BY THIS MANUAL" in General Information of this service manual.

HP Part No. 04291-90111
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Notice

The information contained in this document is subject to change without notice.

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Manual Printing History

The manual printing date and part number indicate its current edition. The printing date changes when a new edition is printed. (Minor corrections and updates that are incorporated at reprint do not cause the date to change.) The manual part number changes when extensive technical changes are incorporated.

January 1998 ..... First Edition

May 1998 ..... Second Edition

Safety Summary

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific *WARNINGS* given elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument.
The Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

Note HP 4291B comply with INSTALLATION CATEGORY II and POLLUTION DEGREE 2 in IEC1010-1. HP 4291B are INDOOR USE product.

Note LEDs in HP 4291B are Class 1 in accordance with IEC825-1.
CLASS 1 LED PRODUCT

Ground The Instrument

This is a Safety Class 1 product (provided with a protective earth terminal). An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and secured against any unintended operation.

DO NOT Operate In An Explosive Atmosphere

Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a safety hazard.

Keep Away From Live Circuits

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with the power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT Service Or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT Substitute Parts Or Modify Instrument

Because of the danger of introducing additional hazards, do not substitute parts or perform unauthorized modifications to the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure the safety features are maintained.

Dangerous Procedure Warnings

Warnings , such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

Warning

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting this instrument.

Typeface Conventions

Bold	Boldface type is used when a term is defined. For example: **icons** are symbols.
Italics	Italic type is used for emphasis and for titles of manuals and other publications. Italic type is also used for keyboard entries when a name or a variable must be typed in place of the words in italics. For example: `copy` *filename* means to type the word `copy`, to type a space, and then to type the name of a file such as `file1`.
`Computer`	Computer font is used for on-screen prompts and messages.
HARDKEYS	Labeled keys on the instrument front panel are enclosed in ▢.
SOFTKEYS	Softkeys located to the right of the LCD are enclosed in ▢.

Safety Symbols

General definitions of safety symbols used on equipment or in manuals are listed below.

Instruction manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the instruction manual.

Alternating current.

Direct current.

On (Supply).

Off (Supply).

In position of push-button switch.

Out position of push-button switch.

Frame (or chassis) terminal. A connection to the frame (chassis) of the equipment which normally include all exposed metal structures.

Warning 

This **Warning** sign denotes a hazard. It calls attention to a procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

Caution 

This **Caution** sign denotes a hazard. It calls attention to a procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

Note 

This **Note** sigh denotes important information. It calls attention to a procedure, practice, condition or the like, which is essential to highlight.

Affixed to product containing static sensitive devices use anti-static handling procedures to prevent electrostatic discharge damage to component.

Certification

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Institute of Standards and Technology, to the extent allowed by the Institution's calibration facility, or to the calibration facilities of other International Standards Organization members.

Warranty

This Hewlett-Packard instrument product is warranted against defects in material and workmanship for a period of one year from the date of shipment, except that in the case of certain components listed in *General Information* of this manual, the warranty shall be for the specified period. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products that prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instruction when property installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

Limitation Of Warranty

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside the environmental specifications for the product, or improper site preparation or maintenance.

No other warranty is expressed or implied. HP specifically disclaims the implied warranties of merchantability and fitness for a particular purpose.

Exclusive Remedies

The remedies provided herein are buyer's sole and exclusive remedies. HP shall not be liable for any direct, indirect, special, incidental, or consequential damages, whether based on contract, tort, or any other legal theory.

Assistance

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

Documentation Map

The following manuals are available for the analyzer:

- **Quick Start Guide(HP Part Number 04291-90021)**

  The *Quick Start Guide* walks you through system setup and initial power-on, shows how to make basic measurements, explains commonly used features, and typical application measurement examples.

- **Operation Manual(HP Part Number 04291-90020)**

  The *Operation Manual* describes all function accessed from the front panel keys and softkeys.It also provides information on option and accessories available and the analyzer features.

- **Programming Manual (HP Part Number 04291-90027)**

  The *Programming Manual* provides information on HP-IB programming.

- **HP Instrument BASIC Users Handbook, (HP Part Number E2083-90005)**

  The *HP Instrument BASIC Users Handbook* introduces you to the HP Instrument BASIC programming language, provides some helpful hints on getting the most use from it, and provides a general programming reference. It is divided into three books, *HP Instrument BASIC Programming Techniques* , *HP Instrument BASIC Interface Techniques* , and *HP Instrument BASIC Language Reference*.

- **Service Manual (Option 0BW only), (HP Part Number 04291-90111)**

  The *Service Manual* explains how to do performance tests, and to adjust, troubleshoot, and repair the instrument.

Contents

13. Replacement Procedures

Figures

Tables

1

General Information

INTRODUCTION

The *Service Manual* is a guide to servicing the HP 4291B RF Impedance/Material Analyzer. The manual contains information required to performance test, adjust, troubleshoot, and repair the analyzer.

ORGANIZATION OF SERVICE MANUAL

This manual consists of the chapters and appendices listed below. They are divided by tabs. This section lists the names of the tabs and the describes content of each chapter and the appendices.

- *Performance Tests.* Provides the procedures required to performance test the analyzer.
- *Adjustments and Correction Constants* . Provides procedures for adjusting the analyzer after repair or replacement of an assembly. Some of the adjustments update the correction constants stored in the EEPROM on the A1 CPU. The correction constants are updated by using the adjustment program (PN 04291-65003).

Note The next six chapters are the troubleshooting chapters.

- *Overall Troubleshooting.* Outlines the analyzer troubleshooting, and provides troubleshooting procedures to isolate the faulty functional group. Faulty assembly isolation procedures for each functional group are contained in the remaining trouble shooting chapters.
- *Power Supply Troubleshooting*
- *Digital Control Troubleshooting*
- *Source Troubleshooting*
- *Receiver Troubleshooting*
- *Transducer Troubleshooting*

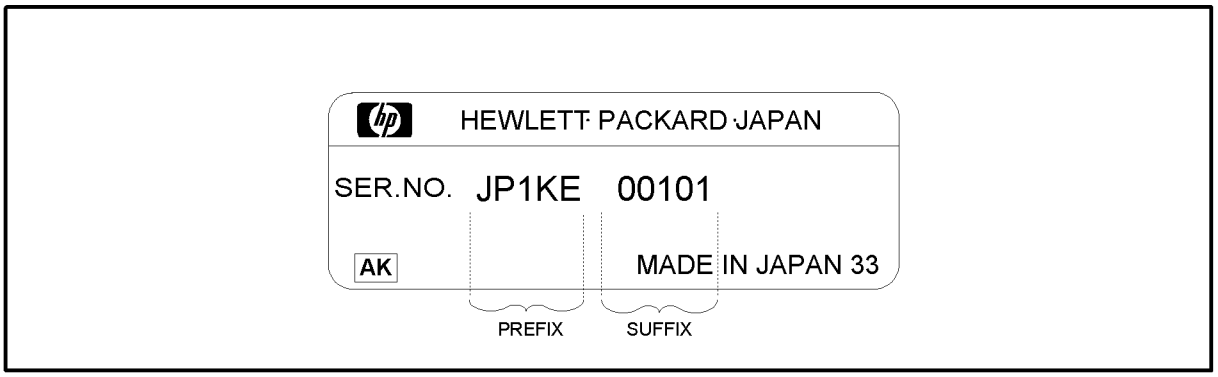
Note The following chapters are, for the most part, reference material.

- *Service Key Menus.* Documents the functions of the menus accessed from (System), `SERVICE MENU` . These menus allow you to test, verify, adjust, control, and troubleshoot the analyzer. HP-IB service mnemonics are included.

- *Theory of Operation.* Explains the overall operation of the analyzer, the division into functional groups, and the operation of each functional group.
- *Replaceable Parts.* Provides part numbers and illustrations of the replaceable assemblies and miscellaneous chassis parts, together with the ordering information.
- *Replacement Procedures.* Provides procedures to disassemble portions of the analyzer when certain assemblies have to be replaced.
- *Post-Repair Procedures.* Contains the table of related service procedures. This is a table of adjustments and verification procedures that must be performed after repair or replacement of each assembly.
- *Appendices.* Contains the manual changes information (required to make this manual compatible with earlier shipment configurations of the analyzer) and the power requirements.
- *Messages.* Contains the service related error message list.

ANALYZERS COVERED BY MANUAL

Hewlett-Packard uses a two-part, ten-character serial number that is stamped on the serial number plate (see Figure 1-1) attached to the rear panel. The first five digits are the serial prefix and the last five digits are the suffix. The same prefix is used for all identical instruments. The prefix changes only when a change is made to the instrument. However, the suffix is assigned sequentially and is unique to each instrument. The contents of this manual apply to instruments with the serial number prefixes listed under **SERIAL NUMBERS** on the title page.



CES0A001

Figure 1-1. Serial Number Plate

An instrument manufactured after the printing date of this manual may have a serial number prefix that is not listed on the title page. This unlisted serial number prefix indicates that the instrument is different from those described in this manual. The manual for an unlisted instrument may be accompanied by a yellow *Manual Changes* supplement or have a different manual part number. The *Manual Changes* supplement contains "change information" that explains how to adapt the manual to newer instruments.

In addition to change information, the supplement may contain information for correcting errors (Errata) in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest *Manual Changes* supplement. The supplement for this manual is identified by this manual's printing data and is available from Hewlett-Packard. If the serial prefix or number of an instrument is lower than that on the title page of this manual, see *Appendix A, Manual Changes*.

For information concerning serial number prefixes not listed on the title page or in the *Manual Changes* supplement, contact the nearest Hewlett-Packard office.

TABLE OF SERVICE TEST EQUIPMENT

The first part of Table 1-1 lists all of the equipment required to performance test, adjust, and troubleshoot the analyzer. The table also notes the use and critical specifications of each item, and the recommended models. Equipment other than the recommended models may be substituted if the equipment meets or exceeds the critical specifications.

In addition to the test equipment listed in Table 1-1, the following tools are also required:

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #1 (small)
- Pozidriv screwdriver, pt size #2 (medium)
- IC extractor
- Open-end wrench, 1/4 inch
- Open-end wrench, 5/16 inch
- Torque wrench, 3/4 inch, 136 N-cm
- Hex socket, 7/32 inch (5.5 mm)
- Flat edge screwdriver

Table 1-1. Recommended Test Equipment

Equipment	Critical Specifications	Recommended Model/ HP Part Number	Qty	Use[1]
Computer	HP 9000 Series 200/300[2]		1	A
BASIC Operating System	Revision 5.0 or above		1	A
Mass Storage	3.5 inch Micro floppy Disk Drive		1	A
Program	HP 4291B Adjustments Program (3.5 inch)	PN 04291-18010	1	A
Performance Test Kit	No substitute	HP 16190A	1	P
Frequency Counter	Frequency Range: 20 MHz to 1 GHz, Time Base Error: $\leq \pm 1.9 \times 10^{-7}$ /year	HP 5343A Opt. 001[3]	1	P, A
Frequency Standard[4]	Frequency: 10 MHz, Time Base Error: $\leq \pm 1 \times 10^{-10}$ /year	HP 5061B	1	A
Spectrum Analyzer	Frequency Range: 100 kHz to 4 GHz	HP 8566A/B	1	A, T
Power Meter	No substitute	HP 436A Opt. 022, HP 437B, or HP 438A	1	P, A
Power Sensor	Frequency Range: 20 MHz to 1.8 GHz, Power: +5 dBm to −20 dBm	HP 8482A	1	P, A
Multimeter	Voltage Range: −40 Vdc to +40 Vdc Voltage Accuracy: <±0.02% Current Range: −100 mAdc to 100 mAdc Current Accuracy: <±0.1%	HP 3458A	1	P, A
Oscilloscope	Band width ≥ 100 MHz	HP 54111D	1	T
Oscilloscope Probe	Impedance: 1 MΩ	HP 10431A	1	T

1 P: Performance Tests, A: Adjustments and Correction Constants, T: Troubleshooting

2 Excluding HP 9826A

3 Option 001 (optional time base) is required for performance testing an analyzer equipped with option 1D5.

4 Required for adjusting an analyzer equipped with Option 1D5.

Table 1-1. Recommended Test Equipment (continued)

Equipment	Critical Specifications	Recommended Model/ HP Part Number	Qty	Use[1]
Cables	TRD cable	PN 04291-65001	1	T
	Type-N cable, 50 Ω	HP 11500B or part of HP 11851B[1]	4	A, T
	BNC cable, 61 cm, 50 Ω	PN 8120-1839	3	P, A, T
	BNC cable, 122 cm, 50 Ω	PN 8120-1840	2	P, A, T
	HP-IB cable	HP 10833A/B/C	3	A
	BNC(f)-SMA(f) adapter, 50 Ω	PN 1250-0562	1	P, A
	SMC(f)-BNC(f) adapter, 50 Ω	PN 1250-0832	1	A
	SMB(f)-BNC(f) adapter, 50 Ω	PN 1250-1236	1	A
	N(m)-BNC(f) adapter, 50 Ω	PN 1250-1476	2	P, A, T
	SMA(m)-BNC(f) adapter, 50 Ω	PN 1250-1548	1	T
	SMA(m)-SMA(f) right angle adapter, 50 Ω	PN 1250-1741	1	T
	APC3.5(m)-APC3.5(f) adapter, 50 Ω	PN 1250-1866	1	P, A
	APC7-N(f) adapter, 50 Ω	HP 11524A or part of HP 85032B[2]	1	P
	BNC(f)-SMA(m) adapter 50 Ω	PN 1250-1548	1	A
	BNC(f)-Banana adapter	PN 1251-2277	1	P, A

1 The HP 11851B includes three N(m)-N(m) cables of 61 cm and a N(m)-N(m) cable of 88 cm.

2 The HP 85032B includes two APC7-N(f) adapters.

2

Performance Tests

INTRODUCTION

This chapter provides the HP 4291B RF Impedance/Material Analyzer performance tests. These performance tests are used to verify that the analyzer's performance meets its specifications.

General information about the performance tests is provided first. Then, step by step procedures for each test are provided.

The each test procedure consists of the following parts:

Description:	Describes the test procedure.
Specification:	Describes the performance verified in the test.
Test Equipment:	Describes test equipment required in the test.
Procedure:	Describes the test procedure step by step.

GENERAL INFORMATION

This section provides general information about the performance tests.

Warm Up Time

Allow the analyzer to warm up for at least 30 minutes before you execute any of the performance tests.

Ambient Conditions

Perform all performance tests in ambient conditions of 23 ± 5°C, ≤ 70%RH.

Calibration Cycle

The analyzer requires periodic performance verification to remain in calibration. The frequency of performance verification depends on the operating and environmental conditions under which the analyzer is used. Verify the analyzer's performance at least once a year using the performance tests given in this chapter.

Performance Test Record

The performance test record lists all test points, acceptable test limits, test result entry columns, and measurement uncertainties. The measurement uncertainty shows how accurately the analyzer's specifications are measured and depends on the test equipment used. The listed measurement uncertainties are valid only when the recommended test equipment is used.

The performance test record is provided at the end of this chapter. Use this record as a master to make extra copies for performance testing.

Recommended Test Equipment

Table 1-1 lists the equipment required for performance testing the analyzer. Other equipment may be substituted if the equipment meets or exceeds the critical specifications given in Table 1-1.

FREQUENCY ACCURACY TEST

Description

This test uses a frequency counter to measure the actual frequency of the analyzer stimulus signal when it is tuned to 1 GHz. This test checks the frequency accuracy of the internal frequency reference (or the high stability frequency reference for Option 1D5).

Specification

(See the *Specifications* of *Operating Manual Set* for details.)

Frequency reference
Accuracy
@ 23±5°C ..... < ±10 ppm
Precision frequency reference (Option 1D5)
Accuracy
@ 0°C to 55°C ..... < ±1 ppm

Test Equipment

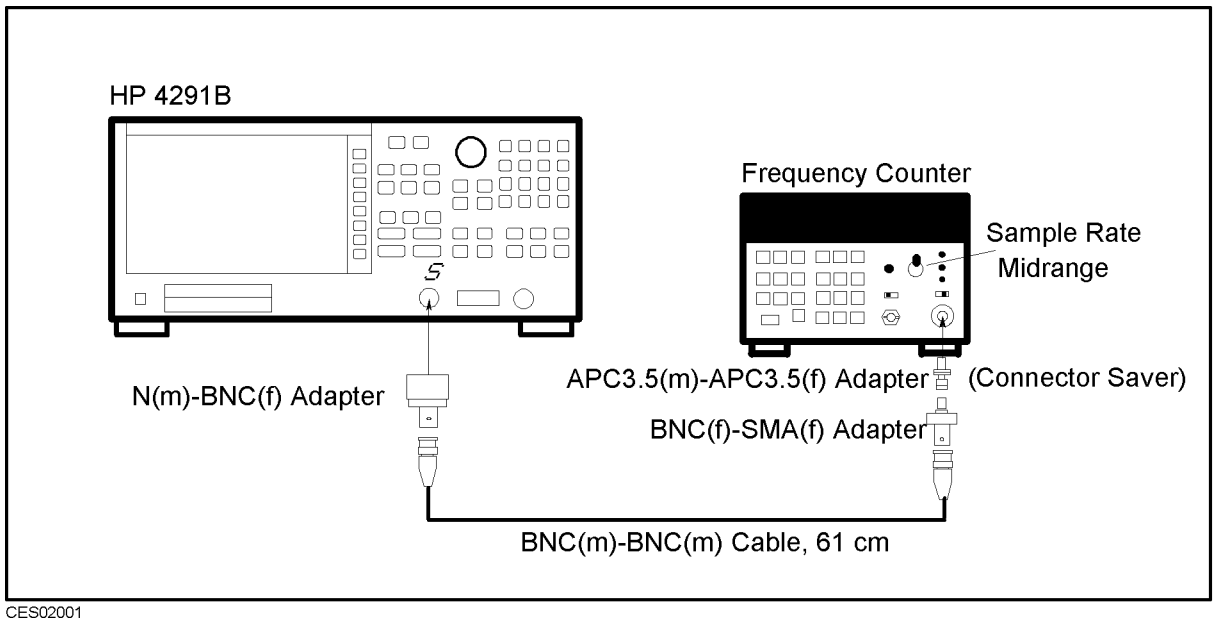
Frequency Counter ..... HP 5343A[1]
BNC cable, 61 cm ..... PN 8120-1839
APC3.5(m)-APC3.5(f) adapter[2] ..... PN 1250-1866
N(m)-BNC(f) adapter ..... PN 1250-1476
BNC(f)-SMA(f) adapter ..... PN 1250-0562

[1]: Option 001 time base is required for testing the analyzer with option 1D5.

[2]: This adapter is used to protect the HP 5343A's APC 3.5 Input connector (it is sometimes called a "connector saver"). In the test setup, the BNC(m)-SMA(f) adapter is connected to the HP 5343A's APC 3.5 Input connector through this adapter. For more information on microwave connectors and connector care, see *MICROWAVE CONNECTOR CARE* (PN 08510-90064).

Procedure

1. Connect the test equipment as shown in Figure 2-1. For testing the analyzer equipped with Option 1D5, connect a BNC(m)-BNC(m) cable between the EXT REF Input connector and the REF OVEN connector on the analyzer rear panel.



CES02001

Figure 2-1. Frequency Accuracy Test Setup

Note

An APC3.5(m)-APC3.5(f) adapter is used between the BNC(f)-SMA(f) adapter and the HP 5343A's APC 3.5 Input connector to protect the HP 5343A's APC 3.5 Input connector. In Figure 2-1, the SMA connector of the BNC(f)-SMA(f) adapter is mated with the APC 3.5 connector of a different type.

2. Initialize the frequency counter. Then set the controls as follows:

Controls	Settings
Sample Rate	Midrange
Range Switch	500 MHz-26.5 MHz
INT/EXT Switch (rear panel)	Internal

3. Press [Preset] to initialize the analyzer. Then set the controls as follows:

Control Settings	Keystrokes
Frequency Span: ZERO	[Span], [0], [x1]
Center Frequency: 1 GHz	[Center], [1], [G/n]
OSC Level: 0.2 V	[Source], [.], [2], [x1]

4. Wait for the frequency counter reading to settle.
5. Subtract 1 GHz (analyzer setting) from the frequency counter reading, and record the result on the performance test record.

OSC LEVEL ACCURACY TEST

Description

This test uses a power meter and a power sensor to measure the actual power level of the stimulus signal at several frequencies from 1 MHz to 1.8 GHz.

Specification

(See the *Specifications* of *Operating Manual Set* for details.)

OSC level accuracy ..... $A + B + \frac{6[dB] \times f[MHz]}{1800}$

where,

A depends on temperature conditions as follows:

when referenced to 23±5°C ..... 2 dB

@ other environmental temperature conditions ..... 4 dB

B depends on OSC level as follows:

@ $P_{osc} \geq -5$ dBm ..... 0 dB

@ -5 dBm $> P_{osc} \geq -45$ dBm ..... 1 dB

@ other OSC levels ..... 2 dB

Test Equipment

Power Meter ..... HP 436A Opt. 022, HP 437B, or HP 438A

Power Sensor ..... HP 8482A

APC-7®-N(f) Adapter ..... HP 11524A

Fixture Stand (only for High Temp. Test Heads) ..... PN 04291-60121

Test Stage Stand (only for High Temp. Test Heads) ..... PN 04291-65021

Extension Rod (only for High Temp. Test Heads) ..... PN 04291-65022

Procedure

Note

The OSC level accuracy test must be done for all test heads attached to the analyzer because the test head characteristics affect the OSC level. The following test procedure is common for all test heads.

1. Connect the power sensor to the power meter. Calibrate the power meter for the power sensor.
2. Connect the test equipment as shown in Figure 2-2.

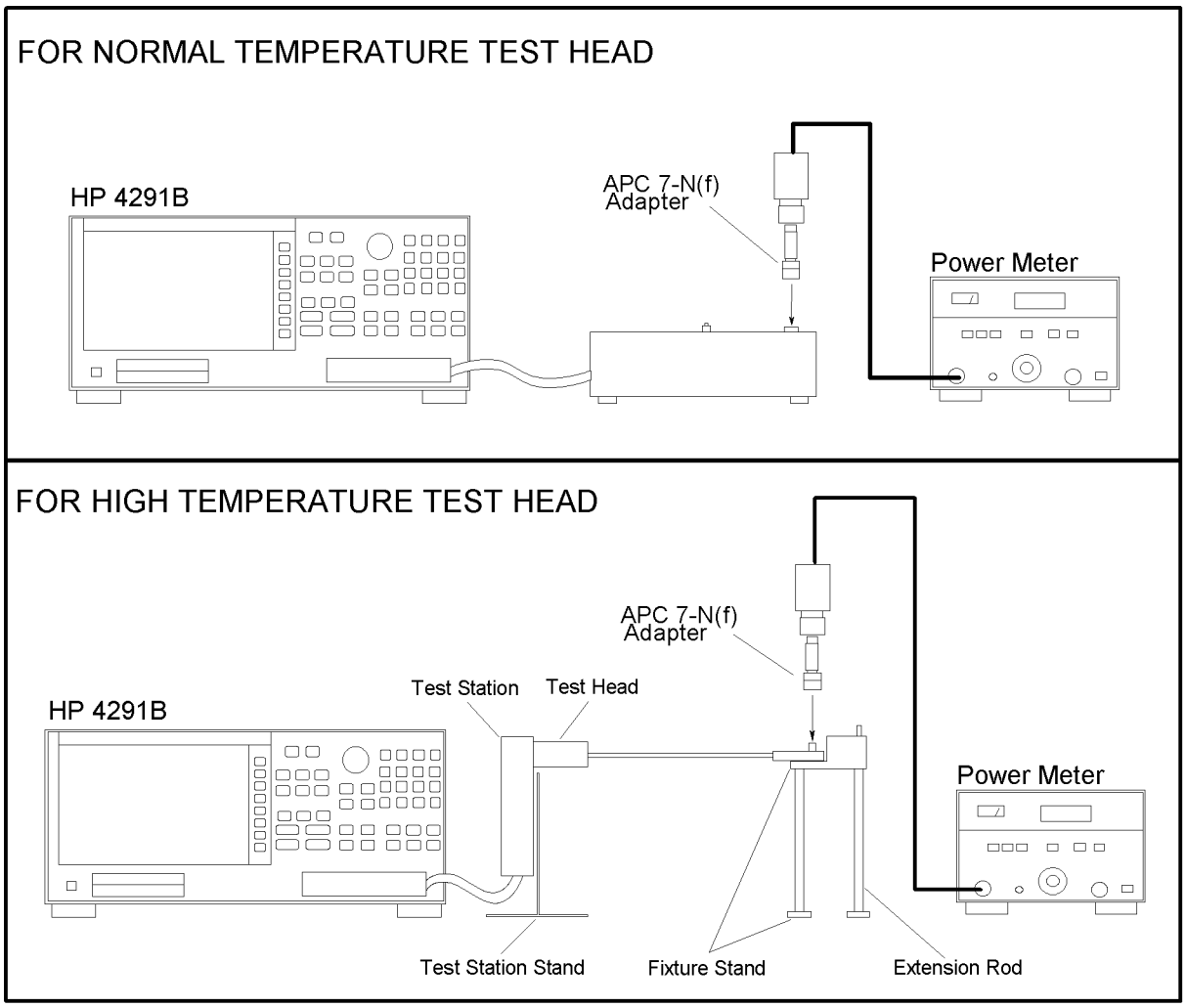


Figure 2-2. OSC Level Accuracy Test Setup

3. Press (Preset) to initialize the HP 4291B.
4. Press (Source), OSC UNIT, dBm to set the OSC level unit to dBm.
5. Set the controls as follows:

Control Settings	Key Strokes
Frequency Span: 0 Hz	(Span), (0), (x1)
Center Frequency: 1 MHz	(Center), (1), (M/μ)
OSC Level: −19 dBm	(Source), (−), (1), (9), (x1)

6. Subtract −19 dBm (analyzer setting) from the power meter reading, and record the result on the performance test record.

7. Change the analyzer OSC level and frequency settings, using `OSC LEVEL`, `Center`, and the numeric keys to test the analyzer at the following test points:

Table 2-1. Test Setting for Normal Temperature Test Heads

OSC Level	Center Freq.
−19 dBm	1 MHz
−13 dBm	10 MHz
−7 dBm	100 MHz
1 dBm	1.8 GHz
7 dBm	1 GHz

Table 2-2. Test Setting for High Temperature Test Heads

OSC Level	Center Freq.	OSC Level	Center Freq.
−19 dBm	1 MHz	−7 dBm	100 MHz
−19 dBm	15 MHz	−7 dBm	200 MHz
−19 dBm	200 MHz	−7 dBm	300 MHz
−19 dBm	300 MHz	−7 dBm	500 MHz
−19 dBm	500 MHz	−7 dBm	800 MHz
−19 dBm	800 MHz	−7 dBm	1 GHz
−19 dBm	1.2 GHz	−7 dBm	1.2 GHz
−19 dBm	1.5 GHz	−7 dBm	1.5 GHz
−13 dBm	10 MHz	−7 dBm	1.8 GHz
−7 dBm	1 MHz	1 dBm	1 MHz
−7 dBm	10 MHz	1 dBm	1 GHz
−7 dBm	15 MHz		

MEASUREMENT ACCURACY TEST

Description

In this test, calibrated standards (from the HP 16190A Performance Test Kit) are measured with the analyzer. Then the analyzer measurement values are compared with the standards' calibration values.

Specification

(See the *Specifications* of *Operating Manual Set* for details.)

Measurement Accuracy ..... Basic Accuracy: 0.8%

Test Equipment

Performance Test Kit ..... HP 16190A
3/4 inch Torque Wrench, 136 N-cm ..... PN 8710-1766
Fixture Stand (only for High Temp. Test Heads) ..... PN 04291-60121
Test Stage Stand (only for High Temp. Test Heads) ..... PN 04291-65021
Extension Rod (only for High Temp. Test Heads) ..... PN 04291-65022

Procedure

Note

Measurement accuracy test must be done for all test heads attached to the analyzer because the test head characteristics affect the measurement. The following test procedure is common for all test heads.

Save the Analyzer Setup

Note

The five calibrated standards are measured in the measurement accuracy test. The analyzer setup for the test is saved, and recalled in each standard measurement to reduce setup time. The two setups for each test head of 400 mV/250 mV setup and 41 mV setup are saved. This saving procedure can be skipped, if the status is already saved.

1. Connect the test equipment as shown in Figure 2-3.

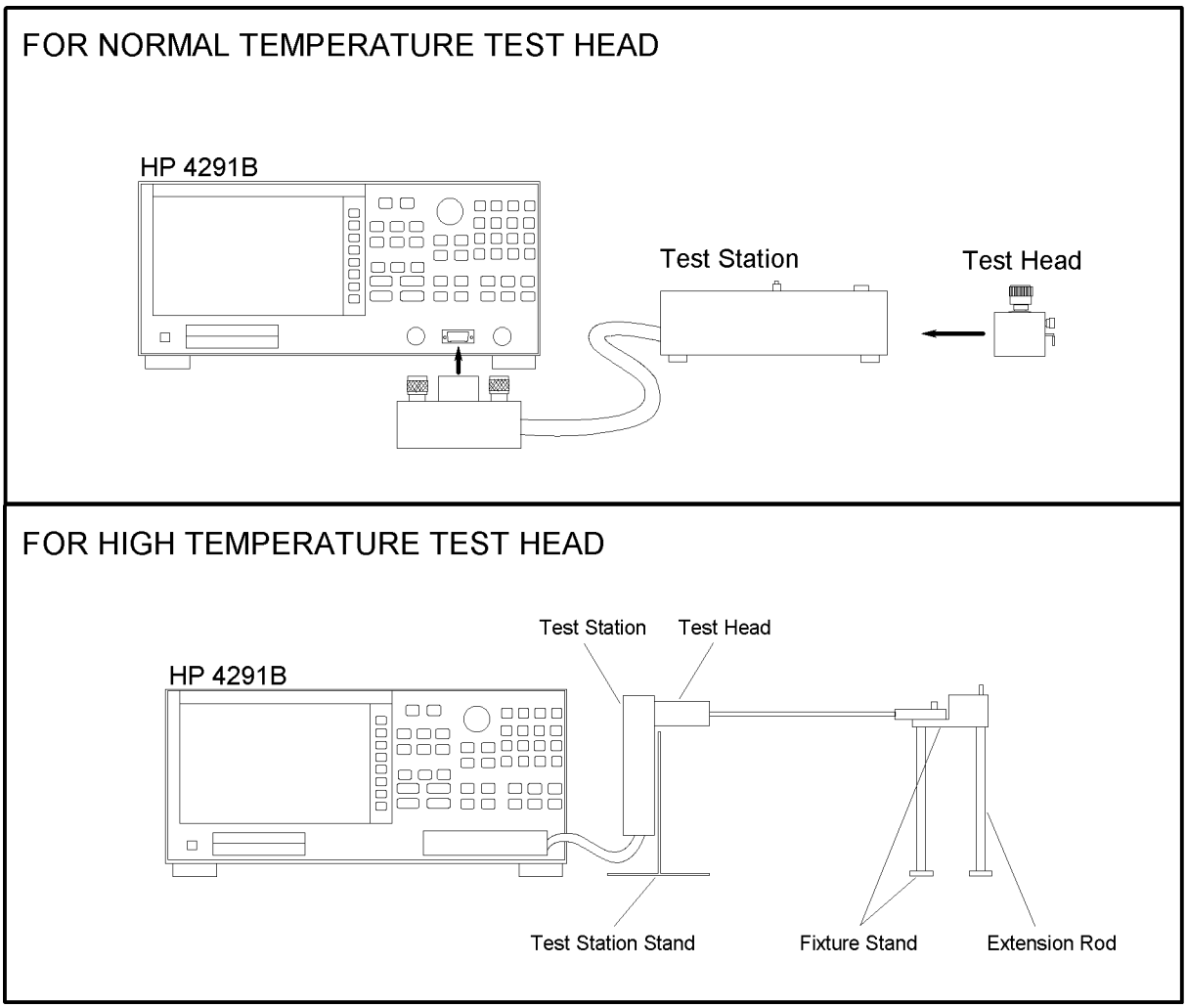


Figure 2-3. Measurement Accuracy Test Setup

2. Press (Preset) to initialize the analyzer.
3. Press (Sweep), `LIST MENU`, `EDIT LIST` to call the sweep list editor.
4. Create the sweep list shown in Figure 2-4, using the following procedure:

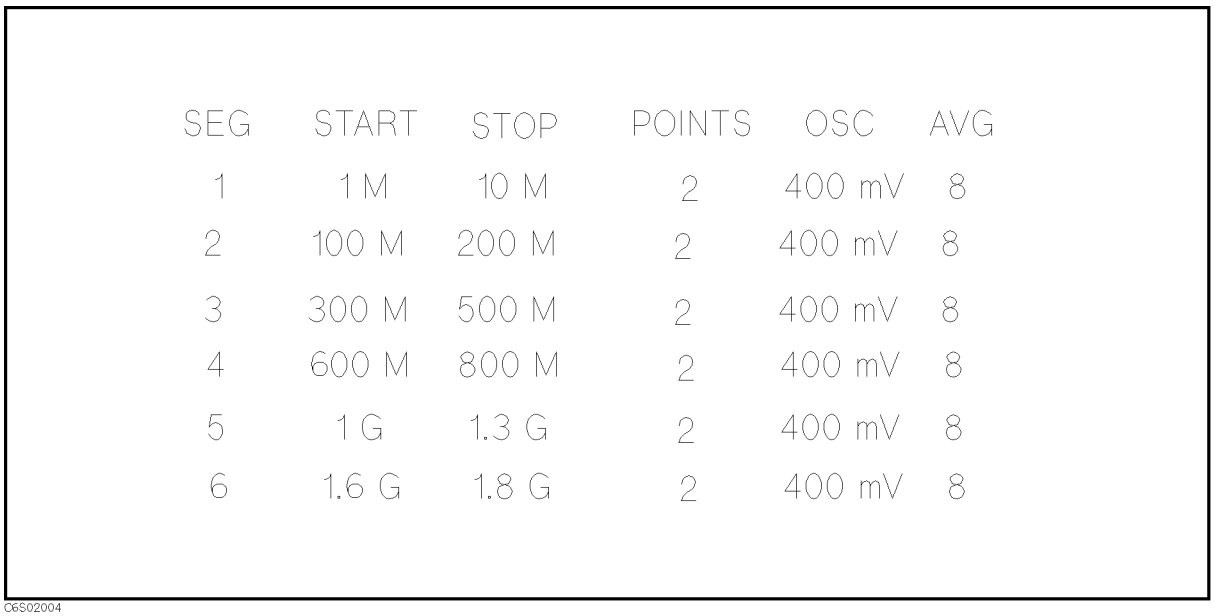


Figure 2-4. Sweep List for Measurement Accuracy Test

a. Press `EDIT`. Then if the normal temperature test head is connected, edit the first segment as follows:

Control Settings	**Key Strokes**
Stop Frequency: 10 MHz	(Stop), (1), (0), (M/μ)
OSC Level: 400 mV	`OSC LEVEL`, (4), (0), (0), (k/m) for normal temperature test heads
Averaging on Point: 8	`AVERAGING ON POINT`, (8), (x1)

b. If the high temperature test head is connected, edit the first segment as follows;

Control Settings	**Key Strokes**
Stop Frequency: 10 MHz	(Stop), (1), (0), (M/μ)
OSC Level: 250 mV	`OSC LEVEL`, (2), (5), (0), (k/m) for high temperature test heads
Averaging on Point: 8	`AVERAGING ON POINT`, (8), (x1)

c. Press `SEGMENT DONE` to store the segment.

d. Press `ADD` to display the second segment. Then edit the segment in the same manner.

e. Edit all the necessary segments. Then press `LIST DONE` to complete the sweep list.

5. Press (Sweep), `SWEEP MENU`, `LIST` to activate the list sweep.

6. Press (Ch2), (Format), and toggle `PHASE UNIT [DEG]` to `PHASE UNIT [RAD]` to set the phase unit of channel 2 to rad.

7. Press (Ch1) to activate channel 1.

8. Press (Save) to enter the save menu.
9. Toggle STOR DEV [DISK] or STOR DEV [MEMORY] to select the storage device. DISK is recommended because the internal memory data is lost when the analyzer power is off.
10. Press STATE to select status save.
11. Save the status as;
    - When the Normal Temperature Test Head is connected, press (4), (0), (0), DONE to save the status with a file name of "400.STA". (The setup for the test at 400 mV OSC level is now saved.)
    - When the High Temperature Test Head is connected, press (2), (5), (0), DONE to save the status with a file name of "250.STA". (The setup for the test at 250 mV OSC level is now saved.)
12. Press (Sweep), LIST MENU, EDIT LIST to call the sweep list editor.
13. Change all OSC level settings to 41 mV, using the following procedure:
    a. Press SEGMENT, (1), (x1) to select the first segment.
    b. Press EDIT to edit the segment.
    c. Press OSC LEVEL, (4), (1), (k/m) to set the OSC level to 41 mV.
    d. Press SEGMENT DONE to store the segment.
    e. Edit the other segments in the same manner.
    f. Press LIST DONE to complete the sweep list.
14. Press (Save) to enter the save menu.
15. Press STATE to select status only save.
16. Press (4), (1), DONE to save the status with a file name of "41.STA". (The setup for the test at 41 mV OSC level is now saved.)

Analyzer Calibration

Note

Calibration must be done when the test head is replaced because the calibration data is valid only for the test head used in the calibration.

Calibration must be done when the analyzer is turned ON because the calibration data is erased when turned OFF.

The analyzer furnished calibration kit must be used for calibration. Do not use the HP 16190A performance test kit.

Do not perform the low-loss capacitor calibration because the analyzer performance is specified without the low-loss capacitor calibration.

Calibration must be done for each sweep list setting.

17. Press (Recall), 400.STA (or 250.STA when the High Temperature Test Head is being tested) to recall the sweep list setup.
18. Press (Cal), CALIBRATE MENU to start the calibration.
19. Connect the 0 S termination of the analyzer calibration kit to the test head APC-7® connector. Then press OPEN to do the open calibration.

20. Disconnect the 0 S, and connect the 0 Ω termination, then press SHORT to do the short calibration.
21. Disconnect the 0 Ω, and connect the 50 Ω termination, then press LOAD to do the short calibration.
22. Press DONE CAL to complete the calibration.
23. Press (Save), RE-SAVE FILES, 400.STA (or 250.STA for the High Temperature Test Head) to overwrite the status data with calibration data.
24. Press (Recall), 41.STA to recall the sweep list setup for 41 mV setting.
25. Repeat step list item 18 to list item 22 with 41.STA setting.
26. Press (Save), RE-SAVE FILES, 41.STA to overwrite the status data with calibration data.

Open Measurement Test

27. Record the open termination calibration values on the performance test record.
28. Connect the open termination to the test head APC-7® connector. Then torque the connection to 136 N-cm.
29. Recall the test settings and the calibration data.
    - When the Normal Temperature Test Head is connected, press (Recall), 400.STA to recall the 400 mV settings.
    - When the High Temperature Test Head is connected, press (Recall), 250.STA to recall the 250 mV settings.
30. Press (meas), DUAL PARAMETER, |Y|-θ to set the measurement parameter to |Y|-θ.
31. Press (Trigger), SINGLE to make a measurement.
32. Press (Copy), MORE, LIST VALUES to display the test results.
33. Subtract the open calibrated values from the analyzer "|Y|" display values. Then record the test results on the performance test record.
34. Press (Recall), 41.STA to recall the 41 mV test settings and the calibration data.
35. Press (meas), DUAL PARAMETER, |Y|-θ to set the measurement parameter to |Y|-θ.
36. Press (Trigger), SINGLE to make a measurement.
37. Press (Copy), MORE, LIST VALUES to display the test results.
38. Subtract the open calibrated values from the analyzer "|Y|" display values. Then record the test results on the performance test record.

Short Measurement Test

39. Record the short termination calibration values on the performance test record.
40. Connect the short termination to the test head APC-7® connector. Then torque the connection to 136 N-cm.
41. Recall the test settings and the calibration data.

- When the Normal Temperature Test Head is connected, press (Recall), 400.STA to recall the 400 mV settings.
- When the High Temperature Test Head is connected, press (Recall), 250.STA to recall the 250 mV settings.

42. Press (Trigger), SINGLE to make a measurement.
43. Press (Copy), MORE, LIST VALUES to display the test results.
44. Subtract the open calibrated values from the analyzer "|Z|" display values. Then record the test results on the performance test record.
45. Press (Recall), 41.STA to recall the 41 mV test settings and the calibration data.
46. Press (Trigger), SINGLE to make a measurement.
47. Press (Copy), MORE, LIST VALUES to display the test results.
48. Record the "|Z|" display values on the performance test record.

50 Ω Measurement Test

49. Record the 50 Ω termination calibration values on the performance test record.
50. Connect the 50 Ω termination to the test head APC-7® connector. Then torque the connection to 136 N-cm.
51. Recall the test settings and the calibration data.
    - When the Normal Temperature Test Head is connected, press (Recall), 400.STA to recall the 400 mV settings.
    - When the High Temperature Test Head is connected, press (Recall), 250.STA to recall the 250 mV settings.
52. Press (Trigger), SINGLE to make a measurement.
53. Press (Copy), MORE, LIST VALUES to display the test results.
54. Subtract the 50 Ω calibrated values from the analyzer "|Z|, θ" display values. Then record the test results on the performance test record.
55. Press (Recall), 41.STA to recall the 41 mV test settings and the calibration data.
56. Press (Trigger), SINGLE to make a measurement.
57. Press (Copy), MORE, LIST VALUES to display the test results.
58. Subtract the 50 Ω calibrated values from the analyzer "|Z|, θ" display values. Then record the test results on the performance test record.

10 cm Airline with Open Test

59. Record the 10 cm airline with open termination calibration values on the performance test record.

60. Connect the 10 cm airline and open termination to the test head APC-7® connector, using the following procedure (see Figure 2-5):

    a. Fully retract the threads on the test head APC-7® connector. Then insert the marked side tip of the airline center conductor into the connector center conductor.

    b. Gently cover the airline center conductor with the airline outer conductor, with the HP logo side down. (To prevent damage, do not let the center conductor scrape the edge of the outer conductor.) Mate the outer conductors . Then torque the connection to 136 N-cm. (A 1/2 inch open end wrench may be necessary to hold the airline stationary.)

    c. Gently inserts the airline center conductor into the open termination center conductor. Mate the outer conductors. Then torque the connection to 136 N-cm.

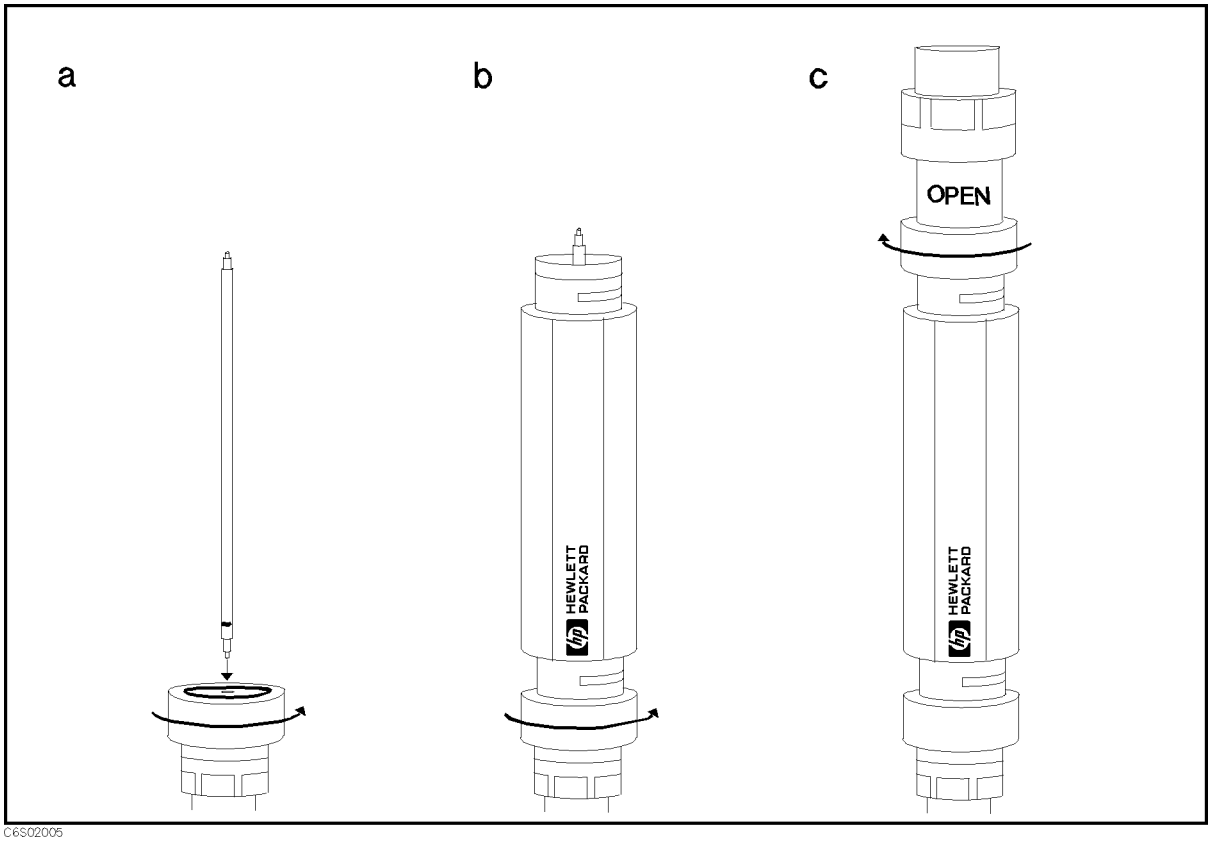


Figure 2-5. 10 cm Airline with Open Measurement Test Setup

61. Recall the test settings and the calibration data.

    - When the Normal Temperature Test Head is connected, press (Recall), `400.STA` to recall the 400 mV settings.
    - When the High Temperature Test Head is connected, press (Recall), `250.STA` to recall the 250 mV settings.

62. Press (Trigger), `SINGLE` to make a measurement.

63. Press (Copy), `MORE` , `LIST VALUES` to display the test results.

64. Subtract the 10 cm airline with open calibrated values from the analyzer "|Z|, θ" display values. Then record the test results on the performance test record. (Ignore the analyzer display values at 1.3 GHz.)

65. Press (Recall), `41.STA` to recall the 41 mV test settings and the calibration data.

66. Press (Trigger), `SINGLE` to make a measurement.

67. Press (Copy), `MORE`, `LIST VALUES` to display the test results.

68. Subtract the 10 cm airline with open calibrated values from the analyzer "|Z|, θ" display values. Then record the test results on the performance test record. (Ignore the analyzer display values at 1.3 GHz.)

10 cm Airline with Short Test

69. Record the 10 cm airline with short termination calibration values on the performance test record.

70. Connect the 10 cm airline and short termination to the test head APC-7® connector, using the following procedure (see Figure 2-6):

    a. Remove the open termination from the airline.

    b. Gently inserts the airline center conductor into the short termination center conductor. Mate the outer conductors. Then torque the connection to 136 N-cm. (A 1/2 inch open end wrench may be necessary to hold the airline stationary .)

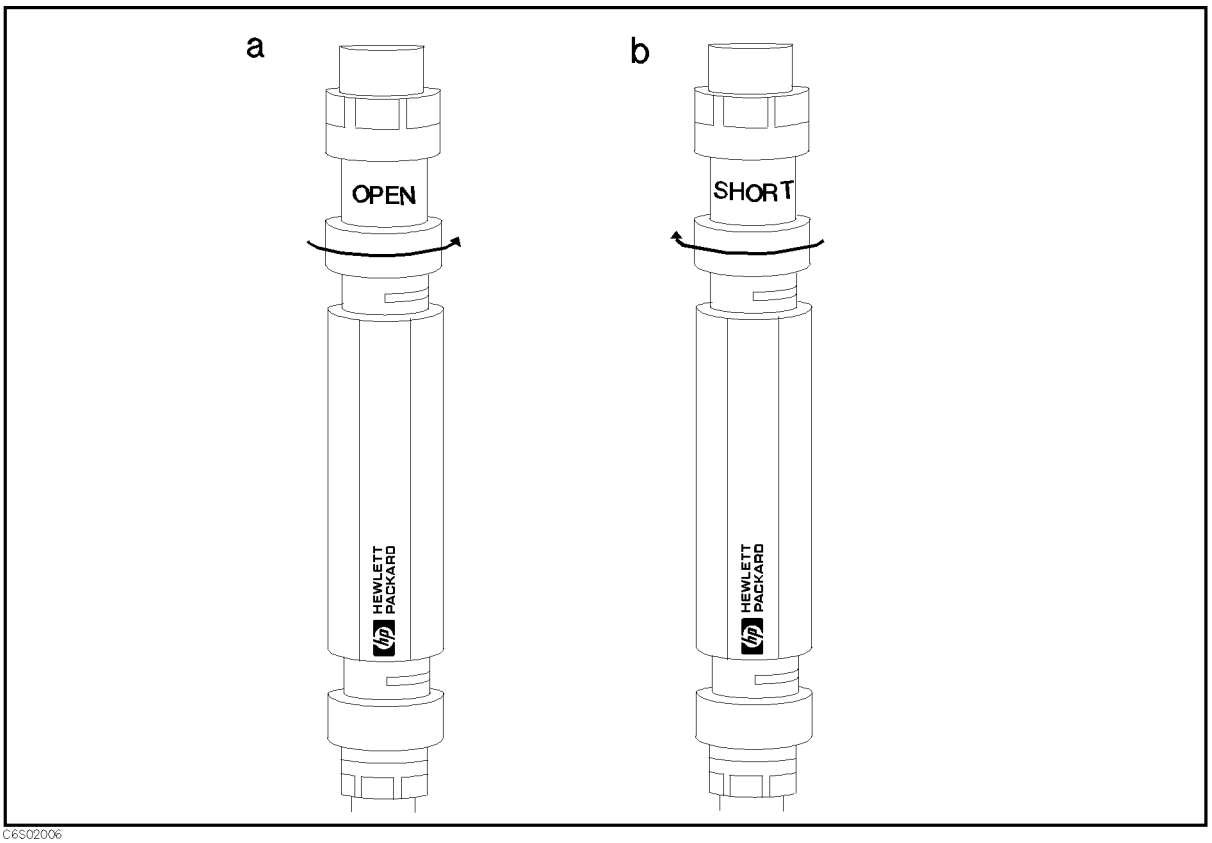


Figure 2-6. 10 cm Airline with Short Measurement Test Setup

71. Recall the test settings and the calibration data.
    - When the Normal Temperature Test Head is connected, press (Recall), `400.STA` to recall the 400 mV settings.
    - When the High Temperature Test Head is connected, press (Recall), `250.STA` to recall the 250 mV settings.
72. Press (Trigger), `SINGLE` to make a measurement.
73. Press (Copy), `MORE`, `LIST VALUES` to display the test results.
74. Subtract the 10 cm airline with short calibrated values from the analyzer "|Z|, θ" display values. Then record the test results on the performance test record. (Ignore the analyzer display values at 800 MHz.)
75. Press (Recall), `41.STA` to recall the 41 mV test settings and the calibration data.
76. Press (Trigger), `SINGLE` to make a measurement.
77. Press (Copy), `MORE`, `LIST VALUES` to display the test results.
78. Subtract the 10 cm airline with short calibrated values from the analyzer "|Z|, θ" display values. Then record the test results on the performance test record. (Ignore the analyzer display values at 800 MHz.)

DC BIAS LEVEL ACCURACY TEST (OPTION 001)

Description

This test uses a multimeter to measure the actual DC bias voltage and current levels of the analyzer.

Specification

(See the *Specifications* of *Operating Manual Set* for details.)

DC bias level accuracy

Voltage (open terminal) ..... 0.1 % + 4 mV
Current (short terminal) ..... 0.5 % + 30 μA

Test Equipment

Multimeter ..... HP 3458A
APC-7®-N(f) Adapter ..... HP 11524A
N(m)-BNC(f) Adapter ..... PN 1250-1476
BNC(f)-Banana Adapter ..... PN 1251-2277
BNC cable, 61 cm ..... PN 8120-1839
Fixture Stand (only for High Temp. Test Heads) ..... PN 04291-60121
Test Stage Stand (only for High Temp. Test Heads) ..... PN 04291-65021
Extension Rod (only for High Temp. Test Heads) ..... PN 04291-65022

Procedure

Note

The DC bias level accuracy test is done for only one test head attached to the analyzer because the test head characteristics don't affect the DC bias level. The following test procedure is common for all test heads.

1. Connect the power sensor to the power meter. Calibrate the power meter for the power sensor.
2. Connect the test equipment as shown in Figure 2-7. The BNC(f)-Banana adapter must be connected to voltage measurement connectors with the "GND" connector connecting to the "LO" terminal.

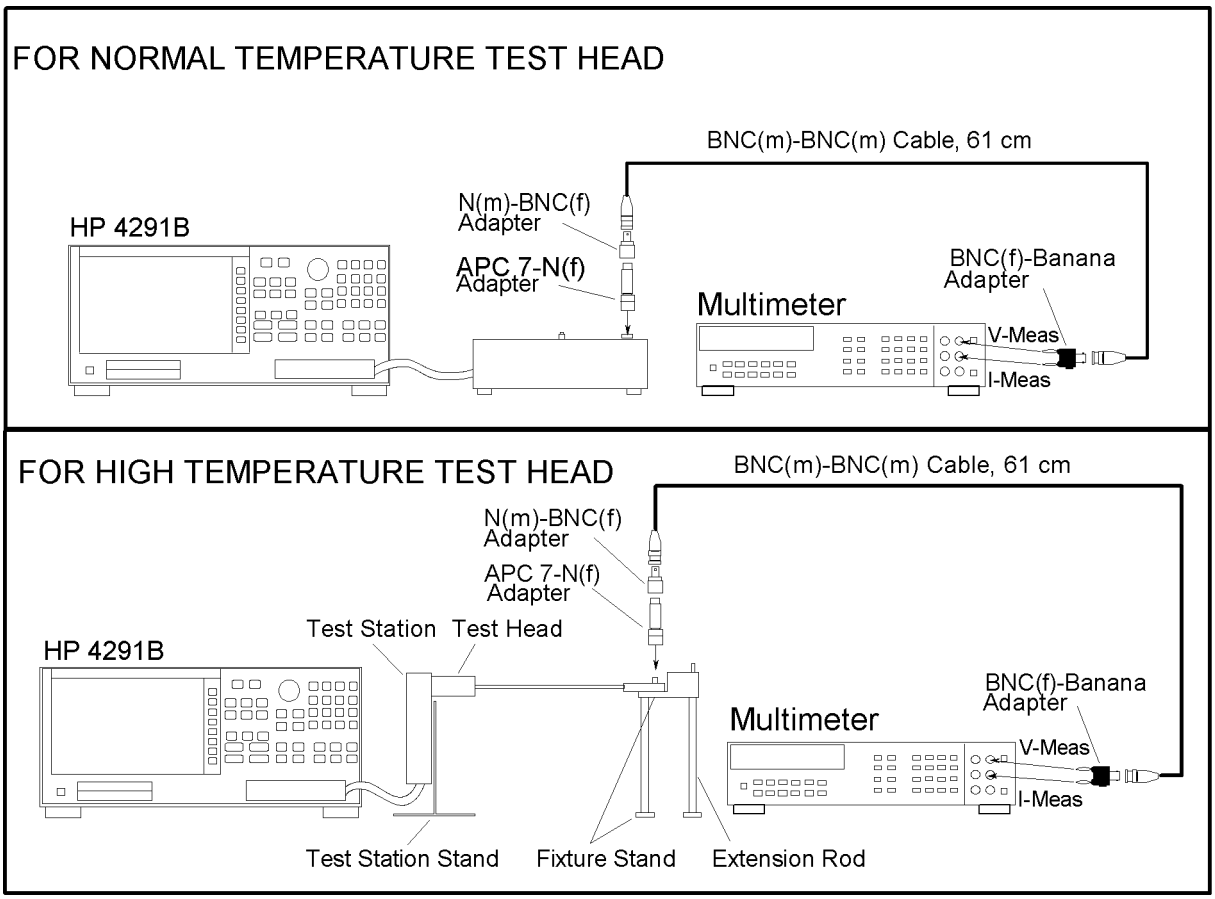


Figure 2-7. DC Bias Level Accuracy Test Setup

3. Initialize the multimeter, then set the NPLC to 100.
4. Press (Preset) to initialize the HP 4291B.
5. Press (Source), (0), (x1) to minimize the OSC level.
6. Toggle `BIAS on OFF` to `BIAS ON off` to turn on the DC bias.
7. Press `DC BIAS MENU`, `BIAS CUR LIMIT`, (1), (0), (0), (k/m) to set the bias current limit to 100 mA.
8. Record the multimeter reading on the 0 V test result column of the performance test record. (The analyzer DC bias voltage is set to 0 V as a preset value.)
9. Press `BIAS VOLTAGE`, (4), (x1) to set the DC bias voltage to 4 V.
10. Subtract 4 V (analyzer setting) from the multimeter reading and record the result on the performance test record.
11. Change the DC bias voltage setting to test the analyzer at the following test points:

Table 2-3. DC Bias Voltage Accuracy Test Settings

Bias Voltage Setting
0 V
4 V
10 V
40 V
– 4 V
– 10 V
– 40 V

12. Toggle `BIAS SRC [VOLTAGE]` to `BIAS SRC [CURRENT]` to set the DC bias current setting mode.
13. Set the multimeter to DCI function and 100 μA range. Then connect the BNC(f)-Banana adapter to current measurement connectors with the "GND" connector connecting to the "LO" terminal.
14. Press `BIAS VOLT LIMIT`, 2, 0, x1 to set the bias voltage limit to 20 V.
15. Record the multimeter reading on the 0 A test result column of the performance test record. (The analyzer DC bias voltage is set to 0 A as a preset value.)
16. Press `BIAS CURRENT`, 2, 0, M/μ, to set the DC bias current to 20 μA.
17. Subtract 20 μA (analyzer setting) from the multimeter reading and record the result on the performance test record.
18. Change the DC bias current setting to test the analyzer at the following test points. The multimeter measurement range must be set to auto mode, except for the 0 A and $\pm$20 μA tests.

Table 2-4. DC Bias Current Accuracy Test Settings

Bias Voltage Setting
0 A
20 μA
1 mA
10 mA
100 mA
–20 μA
–1 mA
–10 mA
–100 mA

PERFORMANCE TEST RECORD

Hewlett-Packard 4291B RF Impedance/Material Analyzer

Serial No. Mainframe _____ Test Date _____

Test Station _____ Temperature _____°C

Norm-Temp High-Z Head _____ Humidity _____%RH

Norm-Temp Low-Z Head _____ Tested by: _____

High-Temp High-Z Head _____

High-Temp Low-Z Head _____

Frequency Accuracy Test

Without Option 1D5

Frequency	Test Limit	Test Result	Measurement Uncertainty
1 GHz	± 10.0 kHz	_____ kHz	±2.3 kHz

With Option 1D5

Frequency	Test Limit	Test Result	Measurement Uncertainty
1 GHz	± 1.00 kHz	_____ kHz	±0.19 kHz

Osc Level Accuracy Test

Norm-Temp High-Impedance Test Head

Osc Level	Frequency	Test Limit	Test Result	Measurement Uncertainty
−19 dBm	1 MHz	±3.00 dB	_____ dB	±0.18 dB
−13 dBm	10 MHz	±3.03 dB	_____ dB	±0.19 dB
−7 dBm	100 MHz	±3.33 dB	_____ dB	±0.20 dB
1 dBm	1.8 GHz	±8.00 dB	_____ dB	±0.19 dB
7 dBm	1 GHz	±5.33 dB	_____ dB	±0.19 dB

Norm-Temp Low-Impedance Test Head (Option 012)

Osc Level	Frequency	Test Limit	Test Result	Measurement Uncertainty
−19 dBm	1 MHz	±3.00 dB	_____ dB	±0.18 dB
−13 dBm	10 MHz	±3.03 dB	_____ dB	±0.19 dB
−7 dBm	100 MHz	±3.33 dB	_____ dB	±0.20 dB
1 dBm	1.8 GHz	±8.00 dB	_____ dB	±0.19 dB
7 dBm	1 GHz	±5.33 dB	_____ dB	±0.19 dB

High-Temp High-Impedance Test Head (Option 013)

Osc Level	Frequency	Test Limit	Test Result	Measurement Uncertainty
−19 dBm	1 MHz	±5.00 dB	_____ dB	±0.22 dB
−19 dBm	15 MHz	±5.07 dB	_____ dB	±0.22 dB
−19 dBm	200 MHz	±5.89 dB	_____ dB	±0.24 dB
−19 dBm	300 MHz	±6.33 dB	_____ dB	±0.24 dB
−19 dBm	500 MHz	±7.22 dB	_____ dB	±0.24 dB
−19 dBm	800 MHz	±8.56 dB	_____ dB	±0.24 dB
−19 dBm	1.2 GHz	±10.33 dB	_____ dB	±0.23 dB
−19 dBm	1.5 GHz	±11.67 dB	_____ dB	±0.23 dB
−13 dBm	10 MHz	±5.04 dB	_____ dB	±0.22 dB
−7 dBm	1 MHz	±4.00 dB	_____ dB	±0.22 dB
−7 dBm	10 MHz	±4.04 dB	_____ dB	±0.22 dB
−7 dBm	15 MHz	±4.07 dB	_____ dB	±0.22 dB
−7 dBm	100 MHz	±4.44 dB	_____ dB	±0.24 dB
−7 dBm	200 MHz	±4.89 dB	_____ dB	±0.24 dB
−7 dBm	300 MHz	±5.33 dB	_____ dB	±0.24 dB
−7 dBm	500 MHz	±6.22 dB	_____ dB	±0.24 dB
−7 dBm	800 MHz	±7.56 dB	_____ dB	±0.24 dB
−7 dBm	1 GHz	±8.44 dB	_____ dB	±0.23 dB
−7 dBm	1.2 GHz	±9.33 dB	_____ dB	±0.23 dB
−7 dBm	1.5 GHz	±10.67 dB	_____ dB	±0.23 dB
−7 dBm	1.8 GHz	±12.00 dB	_____ dB	±0.23 dB
1 dBm	1 MHz	±4.00 dB	_____ dB	±0.22 dB
1 dBm	1 GHz	±8.44 dB	_____ dB	±0.23 dB

High-Temp Low-Impedance Test Head (Option 014)

Osc Level	Frequency	Test Limit	Test Result	Measurement Uncertainty
−19 dBm	1 MHz	±5.00 dB	_____ dB	±0.22 dB
−19 dBm	15 MHz	±5.07 dB	_____ dB	±0.22 dB
−19 dBm	200 MHz	±5.89 dB	_____ dB	±0.24 dB
−19 dBm	300 MHz	±6.33 dB	_____ dB	±0.24 dB
−19 dBm	500 MHz	±7.22 dB	_____ dB	±0.24 dB
−19 dBm	800 MHz	±8.56 dB	_____ dB	±0.24 dB
−19 dBm	1.2 GHz	±10.33 dB	_____ dB	±0.23 dB
−19 dBm	1.5 GHz	±11.67 dB	_____ dB	±0.23 dB
−13 dBm	10 MHz	±5.04 dB	_____ dB	±0.22 dB
−7 dBm	1 MHz	±4.00 dB	_____ dB	±0.22 dB
−7 dBm	10 MHz	±4.04 dB	_____ dB	±0.22 dB
−7 dBm	15 MHz	±4.07 dB	_____ dB	±0.22 dB
−7 dBm	100 MHz	±4.44 dB	_____ dB	±0.24 dB
−7 dBm	200 MHz	±4.89 dB	_____ dB	±0.24 dB
−7 dBm	300 MHz	±5.33 dB	_____ dB	±0.24 dB
−7 dBm	500 MHz	±6.22 dB	_____ dB	±0.24 dB
−7 dBm	800 MHz	±7.56 dB	_____ dB	±0.24 dB
−7 dBm	1 GHz	±8.44 dB	_____ dB	±0.23 dB
−7 dBm	1.2 GHz	±9.33 dB	_____ dB	±0.23 dB
−7 dBm	1.5 GHz	±10.67 dB	_____ dB	±0.23 dB
−7 dBm	1.8 GHz	±12.00 dB	_____ dB	±0.23 dB
1 dBm	1 MHz	±4.00 dB	_____ dB	±0.22 dB
1 dBm	1 GHz	±8.44 dB	_____ dB	±0.23 dB

Measurement Accuracy Test

Norm-Temp High-Impedance Test Head

Test Head: Norm-Temp High-Z
Standard: Open
Osc Level: 400 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Y|	_____ μS	±2.12 μS	_____ μS	±0.03 μS
10 MHz	|Y|	_____ μS	±3.24 μS	_____ μS	±0.34 μS
100 MHz	|Y|	_____ μS	±14.4 μS	_____ μS	±3.4 μS
200 MHz	|Y|	_____ μS	±28.4 μS	_____ μS	±6.7 μS
300 MHz	|Y|	_____ mS	±41.8 μS	_____ μS	±10.0 μS
500 MHz	|Y|	_____ mS	±69.1 μS	_____ μS	±16.7 μS
600 MHz	|Y|	_____ mS	±97.6 μS	_____ μS	±21.3 μS
800 MHz	|Y|	_____ mS	±130 μS	_____ μS	±28 μS
1 GHz	|Y|	_____ mS	±164 μS	_____ μS	±35 μS
1.3 GHz	|Y|	_____ mS	±259 μS	_____ μS	±46 μS
1.6 GHz	|Y|	_____ mS	±329 μS	_____ μS	±63 μS
1.8 GHz	|Y|	_____ mS	±379 μS	_____ μS	±71 μS

Test Head: Norm-Temp High-Z
Standard: Open
Osc Level: 41 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Y|	_____ μS	±20.1 μS	_____ μS	±0.03 μS
10 MHz	|Y|	_____ μS	±21.2 μS	_____ μS	±0.34 μS
100 MHz	|Y|	_____ μS	±32.4 μS	_____ μS	±3.4 μS
200 MHz	|Y|	_____ μS	±46.4 μS	_____ μS	±6.7 μS
300 MHz	|Y|	_____ mS	±59.8 μS	_____ μS	±10.0 μS
500 MHz	|Y|	_____ mS	±87.1 μS	_____ μS	±16.7 μS
600 MHz	|Y|	_____ mS	±111 μS	_____ μS	±21 μS
800 MHz	|Y|	_____ mS	±143 μS	_____ μS	±28 μS
1 GHz	|Y|	_____ mS	±177 μS	_____ μS	±35 μS
1.3 GHz	|Y|	_____ mS	±272 μS	_____ μS	±46 μS
1.6 GHz	|Y|	_____ mS	±342 μS	_____ μS	±63 μS
1.8 GHz	|Y|	_____ mS	±392 μS	_____ μS	±71 μS

Test Head: Norm-Temp High-Z
Standard: Short
Osc Level: 400 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	0.00 mΩ	±101 mΩ	_____ mΩ	±2 mΩ
10 MHz	|Z|	0.00 mΩ	±105 mΩ	_____ mΩ	±2 mΩ
100 MHz	|Z|	0.00 mΩ	±150 mΩ	_____ mΩ	±10 mΩ
200 MHz	|Z|	0.00 mΩ	±200 mΩ	_____ mΩ	±20 mΩ
300 MHz	|Z|	0.00 mΩ	±250 mΩ	_____ mΩ	±30 mΩ
500 MHz	|Z|	0.00 mΩ	±350 mΩ	_____ mΩ	±40 mΩ
600 MHz	|Z|	0.00 mΩ	±400 mΩ	_____ mΩ	±50 mΩ
800 MHz	|Z|	0.00 mΩ	±500 mΩ	_____ mΩ	±70 mΩ
1 GHz	|Z|	0.00 mΩ	±600 mΩ	_____ mΩ	±80 mΩ
1.3 GHz	|Z|	0.00 mΩ	±750 mΩ	_____ mΩ	±100 mΩ
1.6 GHz	|Z|	0.00 mΩ	±900 mΩ	_____ mΩ	±120 mΩ
1.8 GHz	|Z|	0.00 mΩ	±1.00 Ω	_____ Ω	±0.13 Ω

Test Head: Norm-Temp High-Z
Standard: Short
Osc Level: 41 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	0.00 mΩ	±101 mΩ	_____ mΩ	±2 mΩ
10 MHz	|Z|	0.00 mΩ	±105 mΩ	_____ mΩ	±2 mΩ
100 MHz	|Z|	0.00 mΩ	±150 mΩ	_____ mΩ	±10 mΩ
200 MHz	|Z|	0.00 mΩ	±200 mΩ	_____ mΩ	±20 mΩ
300 MHz	|Z|	0.00 mΩ	±250 mΩ	_____ mΩ	±30 mΩ
500 MHz	|Z|	0.00 mΩ	±350 mΩ	_____ mΩ	±40 mΩ
600 MHz	|Z|	0.00 mΩ	±400 mΩ	_____ mΩ	±50 mΩ
800 MHz	|Z|	0.00 mΩ	±500 mΩ	_____ mΩ	±70 mΩ
1 GHz	|Z|	0.00 mΩ	±600 mΩ	_____ mΩ	±80 mΩ
1.3 GHz	|Z|	0.00 mΩ	±750 mΩ	_____ mΩ	±100 mΩ
1.6 GHz	|Z|	0.00 mΩ	±900 mΩ	_____ mΩ	±120 mΩ
1.8 GHz	|Z|	0.00 mΩ	±1.00 Ω	_____ Ω	±0.13 Ω

Test Head: Norm-Temp High-Z
Standard: 50 Ω
Osc Level: 400 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	_____ Ω	±418 mΩ	_____ mΩ	±90 mΩ
1 MHz	θ	_____ mrad	±8.37 mrad	_____ mrad	±1.80 mrad
10 MHz	|Z|	_____ Ω	±425 mΩ	_____ mΩ	±90 mΩ
10 MHz	θ	_____ mrad	±8.50 mrad	_____ mrad	±1.80 mrad
100 MHz	|Z|	_____ Ω	±493 mΩ	_____ mΩ	±100 mΩ
100 MHz	θ	_____ mrad	±9.85 mrad	_____ mrad	±2.00 mrad
200 MHz	|Z|	_____ Ω	±668 mΩ	_____ mΩ	±125 mΩ
200 MHz	θ	_____ mrad	±13.4 mrad	_____ mrad	±2.5 mrad
300 MHz	|Z|	_____ Ω	±743 mΩ	_____ mΩ	±150 mΩ
300 MHz	θ	_____ mrad	±14.9 mrad	_____ mrad	±3.0 mrad
500 MHz	|Z|	_____ Ω	±893 mΩ	_____ mΩ	±200 mΩ
500 MHz	θ	_____ mrad	±17.9 mrad	_____ mrad	±4.0 mrad
600 MHz	|Z|	_____ Ω	±1.17 Ω	_____ Ω	±0.25 Ω
600 MHz	θ	_____ mrad	±23.4 mrad	_____ mrad	±5.0 mrad
800 MHz	|Z|	_____ Ω	±1.32 Ω	_____ Ω	±0.25 Ω
800 MHz	θ	_____ mrad	±26.4 mrad	_____ mrad	±5.0 mrad
1 GHz	|Z|	_____ Ω	±1.47 Ω	_____ Ω	±0.25 Ω
1 GHz	θ	_____ mrad	±29.4 mrad	_____ mrad	±5.0 mrad
1.3 GHz	|Z|	_____ Ω	±2.09 Ω	_____ Ω	±0.25 Ω
1.3 GHz	θ	_____ mrad	±41.9 mrad	_____ mrad	±5.0 mrad
1.6 GHz	|Z|	_____ Ω	±2.32 Ω	_____ Ω	±0.25 Ω
1.6 GHz	θ	_____ mrad	±46.4 mrad	_____ mrad	±5.0 mrad
1.8 GHz	|Z|	_____ Ω	±2.47 Ω	_____ Ω	±0.25 Ω
1.8 GHz	θ	_____ mrad	±49.4 mrad	_____ mrad	±5.0 mrad

Test Head: Norm-Temp High-Z
Standard: 50 Ω
Osc Level: 41 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	_____ Ω	±451 mΩ	_____ mΩ	±90 mΩ
1 MHz	θ	_____ mrad	±9.02 mrad	_____ mrad	±1.80 mrad
10 MHz	|Z|	_____ Ω	±458 mΩ	_____ mΩ	±90 mΩ
10 MHz	θ	_____ mrad	±9.15 mrad	_____ mrad	±1.80 mrad
100 MHz	|Z|	_____ Ω	±525 mΩ	_____ mΩ	±100 mΩ
100 MHz	θ	_____ mrad	±10.5 mrad	_____ mrad	±2.0 mrad
200 MHz	|Z|	_____ Ω	±700 mΩ	_____ mΩ	±125 mΩ
200 MHz	θ	_____ mrad	±14.0 mrad	_____ mrad	±2.5 mrad
300 MHz	|Z|	_____ Ω	±775 mΩ	_____ mΩ	±150 mΩ
300 MHz	θ	_____ mrad	±15.5 mrad	_____ mrad	±3.0 mrad
500 MHz	|Z|	_____ Ω	±925 mΩ	_____ mΩ	±200 mΩ
500 MHz	θ	_____ mrad	±18.5 mrad	_____ mrad	±4.0 mrad
600 MHz	|Z|	_____ Ω	±1.20 Ω	_____ Ω	±0.25 Ω
600 MHz	θ	_____ mrad	±24.0 mrad	_____ mrad	±5.0 mrad
800 MHz	|Z|	_____ Ω	±1.35 Ω	_____ Ω	±0.25 Ω
800 MHz	θ	_____ mrad	±27.0 mrad	_____ mrad	±5.0 mrad
1 GHz	|Z|	_____ Ω	±1.50 Ω	_____ Ω	±0.25 Ω
1 GHz	θ	_____ mrad	±30.0 mrad	_____ mrad	±5.0 mrad
1.3 GHz	|Z|	_____ Ω	±2.13 Ω	_____ Ω	±0.25 Ω
1.3 GHz	θ	_____ mrad	±42.5 mrad	_____ mrad	±5.0 mrad
1.6 GHz	|Z|	_____ Ω	±2.35 Ω	_____ Ω	±0.25 Ω
1.6 GHz	θ	_____ mrad	±47.0 mrad	_____ mrad	±5.0 mrad
1.8 GHz	|Z|	_____ Ω	±2.50 Ω	_____ Ω	±0.25 Ω
1.8 GHz	θ	_____ mrad	±50.0 mrad	_____ mrad	±5.0 mrad

Test Head: Norm-Temp High-Z
Standard: 10 cm Airline with Open
Osc Level: 400 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	_____ kΩ	±1.13 kΩ	_____ kΩ	±0.04 kΩ
1 MHz	θ	_____ rad	±51.8 mrad	_____ mrad	±2.0 mrad
10 MHz	|Z|	_____ kΩ	±27.5 Ω	_____ Ω	±4.4 Ω
10 MHz	θ	_____ rad	±12.6 mrad	_____ mrad	±2.0 mrad
100 MHz	|Z|	_____ Ω	±2.22 Ω	_____ Ω	±0.43 Ω
100 MHz	θ	_____ rad	±10.3 mrad	_____ mrad	±2.0 mrad
200 MHz	|Z|	_____ Ω	±1.29 Ω	_____ Ω	±0.25 Ω
200 MHz	θ	_____ rad	±12.7 mrad	_____ mrad	±2.5 mrad
300 MHz	|Z|	_____ Ω	±874 mΩ	_____ mΩ	±182 mΩ
300 MHz	θ	_____ rad	±14.4 mrad	_____ mrad	±3.0 mrad
500 MHz	|Z|	_____ Ω	±559 mΩ	_____ mΩ	±90 mΩ
500 MHz	θ	_____ rad	±24.8 mrad	_____ mrad	±4.0 mrad
600 MHz	|Z|	_____ Ω	±524 mΩ	_____ mΩ	±88 mΩ
600 MHz	θ	_____ rad	±53.4 mrad	_____ mrad	±9.0 mrad
800 MHz	|Z|	_____ Ω	±679 mΩ	_____ mΩ	±122 mΩ
800 MHz	θ	_____ rad	±50.0 mrad	_____ mrad	±9.0 mrad
1 GHz	|Z|	_____ Ω	±1.34 Ω	_____ Ω	±0.27 Ω
1 GHz	θ	_____ rad	±30.3 mrad	_____ mrad	±6.0 mrad
1.6 GHz	|Z|	_____ Ω	±3.84 Ω	_____ Ω	±0.86 Ω
1.6 GHz	θ	_____ rad	±44.8 mrad	_____ mrad	±10.0 mrad
1.8 GHz	|Z|	_____ Ω	±1.87 Ω	_____ Ω	±0.33 Ω
1.8 GHz	θ	_____ rad	±56.4 mrad	_____ mrad	±10.0 mrad

Test Head: Norm-Temp High-Z
Standard: 10 cm Airline with Open
Osc Level: 41 mV

Frequency	Measurement Parameter	Calibration Value		Test Limit	Test Result		Measurement Uncertainty
1 MHz	|Z|	_____	kΩ	±9.69 kΩ	_____	kΩ	±0.04 kΩ
1 MHz	θ	_____	rad	±444 mrad	_____	mrad	±2 mrad
10 MHz	|Z|	_____	kΩ	±113 Ω	_____	Ω	±4 Ω
10 MHz	θ	_____	rad	±51.8 mrad	_____	mrad	±2.0 mrad
100 MHz	|Z|	_____	Ω	±2.81 Ω	_____	Ω	±0.43 Ω
100 MHz	θ	_____	rad	±13.1 mrad	_____	mrad	±2.0 mrad
200 MHz	|Z|	_____	Ω	±1.42 Ω	_____	Ω	±0.25 Ω
200 MHz	θ	_____	rad	±14.0 mrad	_____	mrad	±2.5 mrad
300 MHz	|Z|	_____	Ω	±922 mΩ	_____	mΩ	±182 mΩ
300 MHz	θ	_____	rad	±15.2 mrad	_____	mrad	±3.0 mrad
500 MHz	|Z|	_____	Ω	±566 mΩ	_____	mΩ	±90 mΩ
500 MHz	θ	_____	rad	±25.1 mrad	_____	mrad	±4.0 mrad
600 MHz	|Z|	_____	Ω	±525 mΩ	_____	mΩ	±88 mΩ
600 MHz	θ	_____	rad	±53.6 mrad	_____	mrad	±9.0 mrad
800 MHz	|Z|	_____	Ω	±682 mΩ	_____	mΩ	±122 mΩ
800 MHz	θ	_____	rad	±50.2 mrad	_____	mrad	±9.0 mrad
1 GHz	|Z|	_____	Ω	±1.37 Ω	_____	Ω	±0.27 Ω
1 GHz	θ	_____	rad	±30.9 mrad	_____	mrad	±6.0 mrad
1.6 GHz	|Z|	_____	Ω	±3.94 Ω	_____	Ω	±0.86 Ω
1.6 GHz	θ	_____	rad	±45.9 mrad	_____	mrad	±10.0 mrad
1.8 GHz	|Z|	_____	Ω	±1.88 Ω	_____	Ω	±0.33 Ω
1.8 GHz	θ	_____	rad	±56.9 mrad	_____	mrad	±10.0 mrad

Test Head: Norm-Temp High-Z
Standard: 10 cm Airline with Short
Osc Level: 400 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	_____ mΩ	±101 mΩ	_____ mΩ	±2 mΩ
1 MHz	θ	_____ rad	±893 mrad	_____ mrad	±15 mrad
10 MHz	|Z|	_____ Ω	±111 mΩ	_____ mΩ	±4 mΩ
10 MHz	θ	_____ rad	±104 mrad	_____ mrad	±4 mrad
100 MHz	|Z|	_____ Ω	±216 mΩ	_____ mΩ	±27 mΩ
100 MHz	θ	_____ rad	±20.2 mrad	_____ mrad	±2.5 mrad
200 MHz	|Z|	_____ Ω	±393 mΩ	_____ mΩ	±67 mΩ
200 MHz	θ	_____ rad	±17.5 mrad	_____ mrad	±3.0 mrad
300 MHz	|Z|	_____ Ω	±592 mΩ	_____ mΩ	±110 mΩ
300 MHz	θ	_____ rad	±16.2 mrad	_____ mrad	±3.0 mrad
500 MHz	|Z|	_____ Ω	±1.48 Ω	_____ Ω	±0.31 Ω
500 MHz	θ	_____ rad	±17.0 mrad	_____ mrad	±3.5 mrad
600 MHz	|Z|	_____ Ω	±3.88 Ω	_____ Ω	±0.78 Ω
600 MHz	θ	_____ rad	±25.0 mrad	_____ mrad	±5.0 mrad
1 GHz	|Z|	_____ Ω	±2.43 Ω	_____ Ω	±0.52 Ω
1 GHz	θ	_____ rad	±28.2 mrad	_____ mrad	±6.0 mrad
1.3 GHz	|Z|	_____ Ω	±1.26 Ω	_____ Ω	±0.22 Ω
1.3 GHz	θ	_____ rad	±57.0 mrad	_____ mrad	±10.0 mrad
1.6 GHz	|Z|	_____ Ω	±1.14 Ω	_____ Ω	±0.16 Ω
1.6 GHz	θ	_____ rad	±105 mrad	_____ mrad	±15 mrad
1.8 GHz	|Z|	_____ Ω	±1.98 Ω	_____ Ω	±0.37 Ω
1.8 GHz	θ	_____ rad	±54.1mrad	_____ mrad	±10.0 mrad

Test Head: Norm-Temp High-Z
Standard: 10 cm Airline with Short
Osc Level: 41 mV

Frequency	Measurement Parameter	Calibration Value		Test Limit	Test Result		Measurement Uncertainty
1 MHz	|Z|	_____	mΩ	±101 mΩ	_____	mΩ	±2 mΩ
1 MHz	θ	_____	rad	±893 mrad	_____	rad	±15 mrad
10 MHz	|Z|	_____	Ω	±111 mΩ	_____	mΩ	±4 mΩ
10 MHz	θ	_____	rad	±104 mrad	_____	mrad	±4 mrad
100 MHz	|Z|	_____	Ω	±218 mΩ	_____	mΩ	±27 mΩ
100 MHz	θ	_____	rad	±20.3 mrad	_____	mrad	±2.5 mrad
200 MHz	|Z|	_____	Ω	±399 mΩ	_____	mΩ	±67 mΩ
200 MHz	θ	_____	rad	±17.8 mrad	_____	mrad	±3.0 mrad
300 MHz	|Z|	_____	Ω	±609 mΩ	_____	mΩ	±110 mΩ
300 MHz	θ	_____	rad	±16.7 mrad	_____	mrad	±3.0 mrad
500 MHz	|Z|	_____	Ω	±1.58 Ω	_____	Ω	±0.31 Ω
500 MHz	θ	_____	rad	±18.1 mrad	_____	mrad	±3.5 mrad
600 MHz	|Z|	_____	Ω	±4.19 Ω	_____	Ω	±0.78 Ω
600 MHz	θ	_____	rad	±27.0 mrad	_____	mrad	±5.0 mrad
1 GHz	|Z|	_____	Ω	±2.52 Ω	_____	Ω	±0.52 Ω
1 GHz	θ	_____	rad	±29.3 mrad	_____	mrad	±6.0 mrad
1.3 GHz	|Z|	_____	Ω	±1.26 Ω	_____	Ω	±0.22 Ω
1.3 GHz	θ	_____	rad	±57.3 mrad	_____	mrad	±10.0 mrad
1.6 GHz	|Z|	_____	Ω	±1.14 Ω	_____	Ω	±0.16 Ω
1.6 GHz	θ	_____	rad	±105 mrad	_____	mrad	±15 mrad
1.8 GHz	|Z|	_____	Ω	±2.00 Ω	_____	Ω	±0.37 Ω
1.8 GHz	θ	_____	rad	±54.6mrad	_____	mrad	±10.0 mrad

Norm-Temp Low-Impedance Test Head (Option 012)

Test Head: Norm-Temp Low-Z
Standard: Open
Osc Level: 400 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Y|	_____ μS	±30.1 μS	_____ μS	±0.0 μS
10 MHz	|Y|	_____ μS	±31.2 μS	_____ μS	±0.3 μS
100 MHz	|Y|	_____ μS	±42.4 μS	_____ μS	±3.4 μS
200 MHz	|Y|	_____ μS	±56.4 μS	_____ μS	±6.7 μS
300 MHz	|Y|	_____ mS	±69.7 μS	_____ μS	±10.0 μS
500 MHz	|Y|	_____ mS	±96.8 μS	_____ μS	±16.7 μS
600 MHz	|Y|	_____ mS	±120 μS	_____ μS	±21 μS
800 MHz	|Y|	_____ mS	±152 μS	_____ μS	±28 μS
1 GHz	|Y|	_____ mS	±185 μS	_____ μS	±35 μS
1.3 GHz	|Y|	_____ mS	±280 μS	_____ μS	±46 μS
1.6 GHz	|Y|	_____ mS	±349 μS	_____ μS	±63 μS
1.8 GHz	|Y|	_____ mS	±398 μS	_____ μS	±71 μS

Test Head: Norm-Temp Low-Z
Standard: Open
Osc Level: 41 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Y|	_____ μS	±30.1 μS	_____ μS	±0.0 μS
10 MHz	|Y|	_____ μS	±31.2 μS	_____ μS	±0.3 μS
100 MHz	|Y|	_____ μS	±42.4 μS	_____ μS	±3.4 μS
200 MHz	|Y|	_____ μS	±56.4 μS	_____ μS	±6.7 μS
300 MHz	|Y|	_____ mS	±69.7 μS	_____ μS	±10.0 μS
500 MHz	|Y|	_____ mS	±96.9 μS	_____ μS	±16.7 μS
600 MHz	|Y|	_____ mS	±120 μS	_____ μS	±21 μS
800 MHz	|Y|	_____ mS	±152 μS	_____ μS	±28 μS
1 GHz	|Y|	_____ mS	±186 μS	_____ μS	±35 μS
1.3 GHz	|Y|	_____ mS	±281 μS	_____ μS	±46 μS
1.6 GHz	|Y|	_____ mS	±350 μS	_____ μS	±63 μS
1.8 GHz	|Y|	_____ mS	±399 μS	_____ μS	±71 μS

Test Head: Norm-Temp Low-Z
Standard: Short
Osc Level: 400 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	0.00 mΩ	±10.5 mΩ	_____ mΩ	±1.8 mΩ
10 MHz	|Z|	0.00 mΩ	±15.0 mΩ	_____ mΩ	±2.0 mΩ
100 MHz	|Z|	0.00 mΩ	±60.0 mΩ	_____ mΩ	±10.0 mΩ
200 MHz	|Z|	0.00 mΩ	±110 mΩ	_____ mΩ	±20 mΩ
300 MHz	|Z|	0.00 mΩ	±160 mΩ	_____ mΩ	±30 mΩ
500 MHz	|Z|	0.00 mΩ	±260 mΩ	_____ mΩ	±40 mΩ
600 MHz	|Z|	0.00 mΩ	±310 mΩ	_____ mΩ	±50 mΩ
800 MHz	|Z|	0.00 mΩ	±410 mΩ	_____ mΩ	±70 mΩ
1 GHz	|Z|	0.00 mΩ	±510 mΩ	_____ mΩ	±80 mΩ
1.3 GHz	|Z|	0.00 mΩ	±660 mΩ	_____ mΩ	±100 mΩ
1.6 GHz	|Z|	0.00 mΩ	±810 mΩ	_____ mΩ	±120 mΩ
1.8 GHz	|Z|	0.00 mΩ	±910 mΩ	_____ mΩ	±130 mΩ

Test Head: Norm-Temp Low-Z
Standard: Short
Osc Level: 41 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	0.00 mΩ	±50.5 mΩ	_____ mΩ	±1.8 mΩ
10 MHz	|Z|	0.00 mΩ	±55.0 mΩ	_____ mΩ	±2.0 mΩ
100 MHz	|Z|	0.00 mΩ	±100 mΩ	_____ mΩ	±10 mΩ
200 MHz	|Z|	0.00 mΩ	±150 mΩ	_____ mΩ	±20 mΩ
300 MHz	|Z|	0.00 mΩ	±200 mΩ	_____ mΩ	±30 mΩ
500 MHz	|Z|	0.00 mΩ	±300 mΩ	_____ mΩ	±40 mΩ
600 MHz	|Z|	0.00 mΩ	±350 mΩ	_____ mΩ	±50 mΩ
800 MHz	|Z|	0.00 mΩ	±450 mΩ	_____ mΩ	±70 mΩ
1 GHz	|Z|	0.00 mΩ	±550 mΩ	_____ mΩ	±80 mΩ
1.3 GHz	|Z|	0.00 mΩ	±700 mΩ	_____ mΩ	±100 mΩ
1.6 GHz	|Z|	0.00 mΩ	±850 mΩ	_____ mΩ	±120 mΩ
1.8 GHz	|Z|	0.00 mΩ	±950 mΩ	_____ mΩ	±130 mΩ

Test Head: Norm-Temp Low-Z
Standard: 50 Ω
Osc Level: 400 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	_____ Ω	±396 mΩ	_____ mΩ	±90 mΩ
1 MHz	θ	_____ mrad	±7.92 mrad	_____ mrad	±1.80 mrad
10 MHz	|Z|	_____ Ω	±403 mΩ	_____ mΩ	±90 mΩ
10 MHz	θ	_____ mrad	±8.05 mrad	_____ mrad	±1.80 mrad
100 MHz	|Z|	_____ Ω	±470 mΩ	_____ mΩ	±100 mΩ
100 MHz	θ	_____ mrad	±9.40 mrad	_____ mrad	±2.00 mrad
200 MHz	|Z|	_____ Ω	±645 mΩ	_____ mΩ	±125 mΩ
200 MHz	θ	_____ mrad	±12.9 mrad	_____ mrad	±2.5 mrad
300 MHz	|Z|	_____ Ω	±720 mΩ	_____ mΩ	±150 mΩ
300 MHz	θ	_____ mrad	±14.4 mrad	_____ mrad	±3.0 mrad
500 MHz	|Z|	_____ Ω	±870 mΩ	_____ mΩ	±200 mΩ
500 MHz	θ	_____ mrad	±17.4 mrad	_____ mrad	±4.0 mrad
600 MHz	|Z|	_____ Ω	±1.15 Ω	_____ Ω	±0.25 Ω
600 MHz	θ	_____ mrad	±22.9 mrad	_____ mrad	±5.0 mrad
800 MHz	|Z|	_____ Ω	±1.30 Ω	_____ Ω	±0.25 Ω
800 MHz	θ	_____ mrad	±25.9 mrad	_____ mrad	±5.0 mrad
1 GHz	|Z|	_____ Ω	±1.45 Ω	_____ Ω	±0.25 Ω
1 GHz	θ	_____ mrad	±28.9 mrad	_____ mrad	±5.0 mrad
1.3 GHz	|Z|	_____ Ω	±2.07 Ω	_____ Ω	±0.25 Ω
1.3 GHz	θ	_____ mrad	±41.4 mrad	_____ mrad	±5.0 mrad
1.6 GHz	|Z|	_____ Ω	±2.30 Ω	_____ Ω	±0.25 Ω
1.6 GHz	θ	_____ mrad	±45.9 mrad	_____ mrad	±5.0 mrad
1.8 GHz	|Z|	_____ Ω	±2.45 Ω	_____ Ω	±0.25 Ω
1.8 GHz	θ	_____ mrad	±48.9 mrad	_____ mrad	±5.0 mrad

Test Head: Norm-Temp Low-Z
Standard: 50 Ω
Osc Level: 41 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	_____ Ω	±426 mΩ	_____ mΩ	±90 mΩ
1 MHz	θ	_____ mrad	±8.52 mrad	_____ mrad	±1.80 mrad
10 MHz	|Z|	_____ Ω	±433 mΩ	_____ mΩ	±90 mΩ
10 MHz	θ	_____ mrad	±8.65 mrad	_____ mrad	±1.80 mrad
100 MHz	|Z|	_____ Ω	±500 mΩ	_____ mΩ	±100 mΩ
100 MHz	θ	_____ mrad	±10.0 mrad	_____ mrad	±2.0 mrad
200 MHz	|Z|	_____ Ω	±675 mΩ	_____ mΩ	±125 mΩ
200 MHz	θ	_____ mrad	±13.5 mrad	_____ mrad	±2.5 mrad
300 MHz	|Z|	_____ Ω	±750 mΩ	_____ mΩ	±150 mΩ
300 MHz	θ	_____ mrad	±15.0 mrad	_____ mrad	±3.0 mrad
500 MHz	|Z|	_____ Ω	±900 mΩ	_____ mΩ	±200 mΩ
500 MHz	θ	_____ mrad	±18.0 mrad	_____ mrad	±4.0 mrad
600 MHz	|Z|	_____ Ω	±1.18 Ω	_____ Ω	±0.25 Ω
600 MHz	θ	_____ mrad	±23.5 mrad	_____ mrad	±5.0 mrad
800 MHz	|Z|	_____ Ω	±1.33 Ω	_____ Ω	±0.25 Ω
800 MHz	θ	_____ mrad	±26.5 mrad	_____ mrad	±5.0 mrad
1 GHz	|Z|	_____ Ω	±1.48 Ω	_____ Ω	±0.25 Ω
1 GHz	θ	_____ mrad	±29.5 mrad	_____ mrad	±5.0 mrad
1.3 GHz	|Z|	_____ Ω	±2.10 Ω	_____ Ω	±0.25 Ω
1.3 GHz	θ	_____ mrad	±42.0 mrad	_____ mrad	±5.0 mrad
1.6 GHz	|Z|	_____ Ω	±2.33 Ω	_____ Ω	±0.25 Ω
1.6 GHz	θ	_____ mrad	±46.5 mrad	_____ mrad	±5.0 mrad
1.8 GHz	|Z|	_____ Ω	±2.48 Ω	_____ Ω	±0.25 Ω
1.8 GHz	θ	_____ mrad	±49.5 mrad	_____ mrad	±5.0 mrad

Test Head: Norm-Temp Low-Z
Standard: 10 cm Airline with Open
Osc Level: 400 mV

Frequency	Measurement Parameter	Calibration Value		Test Limit	Test Result		Measurement Uncertainty
1 MHz	|Z|	_____	kΩ	±14.4 kΩ	_____	kΩ	±0.0 kΩ
1 MHz	θ	_____	rad	±662 mrad	_____	mrad	±2 mrad
10 MHz	|Z|	_____	kΩ	±161 Ω	_____	Ω	±4 Ω
10 MHz	θ	_____	rad	±73.6 mrad	_____	mrad	±2.0 mrad
100 MHz	|Z|	_____	Ω	±3.19 Ω	_____	Ω	±0.43 Ω
100 MHz	θ	_____	rad	±14.9 mrad	_____	mrad	±2.0 mrad
200 MHz	|Z|	_____	Ω	±1.44 Ω	_____	Ω	±0.25 Ω
200 MHz	θ	_____	rad	±14.2 mrad	_____	mrad	±2.5 mrad
300 MHz	|Z|	_____	Ω	±879 mΩ	_____	mΩ	±182 mΩ
300 MHz	θ	_____	rad	±14.4 mrad	_____	mrad	±3.0 mrad
500 MHz	|Z|	_____	Ω	±491 mΩ	_____	mΩ	±90 mΩ
500 MHz	θ	_____	rad	±21.8 mrad	_____	mrad	±4.0 mrad
600 MHz	|Z|	_____	Ω	±446 mΩ	_____	mΩ	±88 mΩ
600 MHz	θ	_____	rad	±45.5 mrad	_____	mrad	±9.0 mrad
800 MHz	|Z|	_____	Ω	±603 mΩ	_____	mΩ	±122 mΩ
800 MHz	θ	_____	rad	±44.4 mrad	_____	mrad	±9.0 mrad
1 GHz	|Z|	_____	Ω	±1.31 Ω	_____	Ω	±0.27 Ω
1 GHz	θ	_____	rad	±29.5 mrad	_____	mrad	±6.0 mrad
1.6 GHz	|Z|	_____	Ω	±3.93 Ω	_____	Ω	±0.86 Ω
1.6 GHz	θ	_____	rad	±45.9 mrad	_____	mrad	±10.0 mrad
1.8 GHz	|Z|	_____	Ω	±1.81 Ω	_____	Ω	±0.33 Ω
1.8 GHz	θ	_____	rad	±54.8 mrad	_____	mrad	±10.0 mrad

Test Head: Norm-Temp Low-Z
Standard: 10 cm Airline with Open
Osc Level: 41 mV

Frequency	Measurement Parameter	Calibration Value		Test Limit	Test Result		Measurement Uncertainty
1 MHz	|Z|	_____	kΩ	±14.4 kΩ	_____	kΩ	±0.0 kΩ
1 MHz	θ	_____	rad	±662 mrad	_____	mrad	±2 mrad
10 MHz	|Z|	_____	kΩ	±161 Ω	_____	Ω	±4 Ω
10 MHz	θ	_____	rad	±73.6 mrad	_____	mrad	±2.0 mrad
100 MHz	|Z|	_____	Ω	±3.22 Ω	_____	Ω	±0.43 Ω
100 MHz	θ	_____	rad	±15.0 mrad	_____	mrad	±2.0 mrad
200 MHz	|Z|	_____	Ω	±1.47 Ω	_____	Ω	±0.25 Ω
200 MHz	θ	_____	rad	±14.5 mrad	_____	mrad	±2.5 mrad
300 MHz	|Z|	_____	Ω	±909 mΩ	_____	mΩ	±182 mΩ
300 MHz	θ	_____	rad	±14.9 mrad	_____	mrad	±3.0 mrad
500 MHz	|Z|	_____	Ω	±521 mΩ	_____	mΩ	±90 mΩ
500 MHz	θ	_____	rad	±23.1 mrad	_____	mrad	±4.0 mrad
600 MHz	|Z|	_____	Ω	±476 mΩ	_____	mΩ	±88 mΩ
600 MHz	θ	_____	rad	±48.6 mrad	_____	mrad	±9.0 mrad
800 MHz	|Z|	_____	Ω	±633 mΩ	_____	mΩ	±122 mΩ
800 MHz	θ	_____	rad	±46.6 mrad	_____	mrad	±9.0 mrad
1 GHz	|Z|	_____	Ω	±1.34 Ω	_____	Ω	±0.27 Ω
1 GHz	θ	_____	rad	±30.2 mrad	_____	mrad	±6.0 mrad
1.6 GHz	|Z|	_____	Ω	±3.96 Ω	_____	Ω	±0.86 Ω
1.6 GHz	θ	_____	rad	±46.2 mrad	_____	mrad	±10.0 mrad
1.8 GHz	|Z|	_____	Ω	±1.84 Ω	_____	Ω	±0.33 Ω
1.8 GHz	θ	_____	rad	±55.7 mrad	_____	mrad	±10.0 mrad

Test Head: Norm-Temp Low-Z
Standard: 10 cm Airline with Short
Osc Level: 400 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	_____ mΩ	±11.2 mΩ	_____ mΩ	±1.7 mΩ
1 MHz	θ	_____ rad	±98.7 mrad	_____ mrad	±15.0 mrad
10 MHz	|Z|	_____ Ω	±21.5 mΩ	_____ mΩ	±4.3 mΩ
10 MHz	θ	_____ rad	±20.0 mrad	_____ mrad	±4.0 mrad
100 MHz	|Z|	_____ Ω	±139 mΩ	_____ mΩ	±27 mΩ
100 MHz	θ	_____ rad	±13.0 mrad	_____ mrad	±2.5 mrad
200 MHz	|Z|	_____ Ω	±324 mΩ	_____ mΩ	±67 mΩ
200 MHz	θ	_____ rad	±14.5 mrad	_____ mrad	±3.0 mrad
300 MHz	|Z|	_____ Ω	±542 mΩ	_____ mΩ	±110 mΩ
300 MHz	θ	_____ rad	±14.8 mrad	_____ mrad	±3.0 mrad
500 MHz	|Z|	_____ Ω	±1.58 Ω	_____ Ω	±0.31 Ω
500 MHz	θ	_____ rad	±18.1 mrad	_____ mrad	±3.5 mrad
600 MHz	|Z|	_____ Ω	±4.35 Ω	_____ Ω	±0.78 Ω
600 MHz	θ	_____ rad	±28.0 mrad	_____ mrad	±5.0 mrad
1 GHz	|Z|	_____ Ω	±2.52 Ω	_____ Ω	±0.52 Ω
1 GHz	θ	_____ rad	±29.2 mrad	_____ mrad	±6.0 mrad
1.3 GHz	|Z|	_____ Ω	±1.19 Ω	_____ Ω	±0.22 Ω
1.3 GHz	θ	_____ rad	±53.9 mrad	_____ mrad	±10.0 mrad
1.6 GHz	|Z|	_____ Ω	±1.06 Ω	_____ Ω	±0.16 Ω
1.6 GHz	θ	_____ rad	±97.8 mrad	_____ mrad	±15.0 mrad
1.8 GHz	|Z|	_____ Ω	±1.94 Ω	_____ Ω	±0.37 Ω
1.8 GHz	θ	_____ rad	±52.8mrad	_____ mrad	±10.0 mrad

Test Head: Norm-Temp Low-Z
Standard: 10 cm Airline with Short
Osc Level: 41 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	_____ mΩ	±51.2 mΩ	_____ mΩ	±1.7 mΩ
1 MHz	θ	_____ rad	±452 mrad	_____ mrad	±15 mrad
10 MHz	|Z|	_____ Ω	±61.5 mΩ	_____ mΩ	±4.3 mΩ
10 MHz	θ	_____ rad	±57.3 mrad	_____ mrad	±4.0 mrad
100 MHz	|Z|	_____ Ω	±169 mΩ	_____ mΩ	±27 mΩ
100 MHz	θ	_____ rad	±15.8 mrad	_____ mrad	±2.5 mrad
200 MHz	|Z|	_____ Ω	±354 mΩ	_____ mΩ	±67 mΩ
200 MHz	θ	_____ rad	±15.8 mrad	_____ mrad	±3.0 mrad
300 MHz	|Z|	_____ Ω	±572 mΩ	_____ mΩ	±110 mΩ
300 MHz	θ	_____ rad	±15.7 mrad	_____ mrad	±3.0 mrad
500 MHz	|Z|	_____ Ω	±1.61 Ω	_____ Ω	±0.31 Ω
500 MHz	θ	_____ rad	±18.4 mrad	_____ mrad	±3.5 mrad
600 MHz	|Z|	_____ Ω	±4.38 Ω	_____ Ω	±0.78 Ω
600 MHz	θ	_____ rad	±28.2 mrad	_____ mrad	±5.0 mrad
1 GHz	|Z|	_____ Ω	±2.55 Ω	_____ Ω	±0.52 Ω
1 GHz	θ	_____ rad	±29.6 mrad	_____ mrad	±6.0 mrad
1.3 GHz	|Z|	_____ Ω	±1.22 Ω	_____ Ω	±0.22 Ω
1.3 GHz	θ	_____ rad	±55.2 mrad	_____ mrad	±10.0 mrad
1.6 GHz	|Z|	_____ Ω	±1.09 Ω	_____ Ω	±0.16 Ω
1.6 GHz	θ	_____ rad	±101 mrad	_____ mrad	±15 mrad
1.8 GHz	|Z|	_____ Ω	±1.97 Ω	_____ Ω	±0.37 Ω
1.8 GHz	θ	_____ rad	±53.6mrad	_____ mrad	±10.0 mrad

High-Temp High-Impedance Test Head (Option 013)

Test Head: High-Temp High-Z
Standard: Open
Osc Level: 250 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Y|	_____ μS	±10.2 μS	_____ μS	±0.0 μS
10 MHz	|Y|	_____ μS	±12.2 μS	_____ μS	±0.3 μS
100 MHz	|Y|	_____ μS	±32.4 μS	_____ μS	±3.4 μS
200 MHz	|Y|	_____ μS	±56.5 μS	_____ μS	±6.7 μS
300 MHz	|Y|	_____ mS	±80.0 μS	_____ μS	±10.0 μS
500 MHz	|Y|	_____ mS	±128 μS	_____ μS	±17 μS
600 MHz	|Y|	_____ mS	±169 μS	_____ μS	±21 μS
800 MHz	|Y|	_____ mS	±226 μS	_____ μS	±28 μS
1 GHz	|Y|	_____ mS	±286 μS	_____ μS	±35 μS
1.3 GHz	|Y|	_____ mS	±460 μS	_____ μS	±46 μS
1.6 GHz	|Y|	_____ mS	±586 μS	_____ μS	±63 μS
1.8 GHz	|Y|	_____ mS	±678 μS	_____ μS	±71 μS

Test Head: High-Temp High-Z
Standard: Open
Osc Level: 41 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Y|	_____ μS	±20.2 μS	_____ μS	±0.0 μS
10 MHz	|Y|	_____ μS	±22.2 μS	_____ μS	±0.3 μS
100 MHz	|Y|	_____ μS	±42.4 μS	_____ μS	±3.4 μS
200 MHz	|Y|	_____ μS	±66.5 μS	_____ μS	±6.7 μS
300 MHz	|Y|	_____ mS	±90.0 μS	_____ μS	±10.0 μS
500 MHz	|Y|	_____ mS	±138 μS	_____ μS	±17 μS
600 MHz	|Y|	_____ mS	±179 μS	_____ μS	±21 μS
800 MHz	|Y|	_____ mS	±236 μS	_____ μS	±28 μS
1 GHz	|Y|	_____ mS	±296 μS	_____ μS	±35 μS
1.3 GHz	|Y|	_____ mS	±470 μS	_____ μS	±46 μS
1.6 GHz	|Y|	_____ mS	±596 μS	_____ μS	±63 μS
1.8 GHz	|Y|	_____ mS	±688 μS	_____ μS	±71 μS

Test Head: High-Temp High-Z
Standard: Short
Osc Level: 250 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	0.00 mΩ	±101 mΩ	_____ mΩ	±2 mΩ
10 MHz	|Z|	0.00 mΩ	±110 mΩ	_____ mΩ	±2 mΩ
100 MHz	|Z|	0.00 mΩ	±200 mΩ	_____ mΩ	±10 mΩ
200 MHz	|Z|	0.00 mΩ	±300 mΩ	_____ mΩ	±20 mΩ
300 MHz	|Z|	0.00 mΩ	±400 mΩ	_____ mΩ	±30 mΩ
500 MHz	|Z|	0.00 mΩ	±600 mΩ	_____ mΩ	±40 mΩ
600 MHz	|Z|	0.00 mΩ	±700 mΩ	_____ mΩ	±50 mΩ
800 MHz	|Z|	0.00 mΩ	±900 mΩ	_____ mΩ	±70 mΩ
1 GHz	|Z|	0.00 mΩ	±1.10 Ω	_____ mΩ	±0.08 Ω
1.3 GHz	|Z|	0.00 mΩ	±1.40 Ω	_____ mΩ	±0.10 Ω
1.6 GHz	|Z|	0.00 mΩ	±1.70 Ω	_____ mΩ	±0.12 Ω
1.8 GHz	|Z|	0.00 mΩ	±1.90 Ω	_____ Ω	±0.13 Ω

Test Head: High-Temp High-Z
Standard: Short
Osc Level: 41 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	0.00 mΩ	±101 mΩ	_____ mΩ	±2 mΩ
10 MHz	|Z|	0.00 mΩ	±110 mΩ	_____ mΩ	±2 mΩ
100 MHz	|Z|	0.00 mΩ	±200 mΩ	_____ mΩ	±10 mΩ
200 MHz	|Z|	0.00 mΩ	±300 mΩ	_____ mΩ	±20 mΩ
300 MHz	|Z|	0.00 mΩ	±400 mΩ	_____ mΩ	±30 mΩ
500 MHz	|Z|	0.00 mΩ	±600 mΩ	_____ mΩ	±40 mΩ
600 MHz	|Z|	0.00 mΩ	±700 mΩ	_____ mΩ	±50 mΩ
800 MHz	|Z|	0.00 mΩ	±900 mΩ	_____ mΩ	±70 mΩ
1 GHz	|Z|	0.00 mΩ	±1.10 Ω	_____ mΩ	±0.08 Ω
1.3 GHz	|Z|	0.00 mΩ	±1.40 Ω	_____ mΩ	±0.10 Ω
1.6 GHz	|Z|	0.00 mΩ	±1.70 Ω	_____ mΩ	±0.12 Ω
1.8 GHz	|Z|	0.00 mΩ	±1.90 Ω	_____ Ω	±0.13 Ω

Test Head: High-Temp High-Z
Standard: 50 Ω
Osc Level: 250 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	_____ Ω	±427 mΩ	_____ mΩ	±90 mΩ
1 MHz	θ	_____ mrad	±8.53 mrad	_____ mrad	±1.80 mrad
10 MHz	|Z|	_____ Ω	±440 mΩ	_____ mΩ	±90 mΩ
10 MHz	θ	_____ mrad	±8.80 mrad	_____ mrad	±1.80 mrad
100 MHz	|Z|	_____ Ω	±575 mΩ	_____ mΩ	±100 mΩ
100 MHz	θ	_____ mrad	±11.5 mrad	_____ mrad	±2.0 mrad
200 MHz	|Z|	_____ Ω	±825 mΩ	_____ mΩ	±125 mΩ
200 MHz	θ	_____ mrad	±16.5 mrad	_____ mrad	±2.5 mrad
300 MHz	|Z|	_____ Ω	±975 mΩ	_____ mΩ	±150 mΩ
300 MHz	θ	_____ mrad	±19.5 mrad	_____ mrad	±3.0 mrad
500 MHz	|Z|	_____ Ω	±1.28 Ω	_____ mΩ	±0.20 Ω
500 MHz	θ	_____ mrad	±25.5 mrad	_____ mrad	±4.0 mrad
600 MHz	|Z|	_____ Ω	±1.78 Ω	_____ Ω	±0.25 Ω
600 MHz	θ	_____ mrad	±35.5 mrad	_____ mrad	±5.0 mrad
800 MHz	|Z|	_____ Ω	±2.08 Ω	_____ Ω	±0.25 Ω
800 MHz	θ	_____ mrad	±41.5 mrad	_____ mrad	±5.0 mrad
1 GHz	|Z|	_____ Ω	±2.38 Ω	_____ Ω	±0.25 Ω
1 GHz	θ	_____ mrad	±47.5 mrad	_____ mrad	±5.0 mrad
1.3 GHz	|Z|	_____ Ω	±3.58 Ω	_____ Ω	±0.25 Ω
1.3 GHz	θ	_____ mrad	±71.5 mrad	_____ mrad	±5.0 mrad
1.6 GHz	|Z|	_____ Ω	±4.03 Ω	_____ Ω	±0.25 Ω
1.6 GHz	θ	_____ mrad	±80.5 mrad	_____ mrad	±5.0 mrad
1.8 GHz	|Z|	_____ Ω	±4.33 Ω	_____ Ω	±0.25 Ω
1.8 GHz	θ	_____ mrad	±86.5 mrad	_____ mrad	±5.0 mrad

Test Head: High-Temp High-Z
Standard: 50 Ω
Osc Level: 41 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	_____ Ω	±452 mΩ	_____ mΩ	±90 mΩ
1 MHz	θ	_____ mrad	±9.03 mrad	_____ mrad	±1.80 mrad
10 MHz	|Z|	_____ Ω	±465 mΩ	_____ mΩ	±90 mΩ
10 MHz	θ	_____ mrad	±9.30 mrad	_____ mrad	±1.80 mrad
100 MHz	|Z|	_____ Ω	±600 mΩ	_____ mΩ	±100 mΩ
100 MHz	θ	_____ mrad	±12.0 mrad	_____ mrad	±2.0 mrad
200 MHz	|Z|	_____ Ω	±850 mΩ	_____ mΩ	±125 mΩ
200 MHz	θ	_____ mrad	±17.0 mrad	_____ mrad	±2.5 mrad
300 MHz	|Z|	_____ Ω	±1.00 Ω	_____ mΩ	±0.15 Ω
300 MHz	θ	_____ mrad	±20.0 mrad	_____ mrad	±3.0 mrad
500 MHz	|Z|	_____ Ω	±1.30 Ω	_____ mΩ	±0.20 Ω
500 MHz	θ	_____ mrad	±26.0 mrad	_____ mrad	±4.0 mrad
600 MHz	|Z|	_____ Ω	±1.80 Ω	_____ Ω	±0.25 Ω
600 MHz	θ	_____ mrad	±36.0 mrad	_____ mrad	±5.0 mrad
800 MHz	|Z|	_____ Ω	±2.10 Ω	_____ Ω	±0.25 Ω
800 MHz	θ	_____ mrad	±42.0 mrad	_____ mrad	±5.0 mrad
1 GHz	|Z|	_____ Ω	±2.40 Ω	_____ Ω	±0.25 Ω
1 GHz	θ	_____ mrad	±48.0 mrad	_____ mrad	±5.0 mrad
1.3 GHz	|Z|	_____ Ω	±3.60 Ω	_____ Ω	±0.25 Ω
1.3 GHz	θ	_____ mrad	±72.0 mrad	_____ mrad	±5.0 mrad
1.6 GHz	|Z|	_____ Ω	±4.05 Ω	_____ Ω	±0.25 Ω
1.6 GHz	θ	_____ mrad	±81.0 mrad	_____ mrad	±5.0 mrad
1.8 GHz	|Z|	_____ Ω	±4.35 Ω	_____ Ω	±0.25 Ω
1.8 GHz	θ	_____ mrad	±87.0 mrad	_____ mrad	±5.0 mrad

Test Head: High-Temp High-Z
Standard: 10 cm Airline with Open
Osc Level: 250 mV

Frequency	Measurement Parameter	Calibration Value		Test Limit	Test Result		Measurement Uncertainty
1 MHz	|Z|	_____	kΩ	±4.98 kΩ	_____	kΩ	±0.04 kΩ
1 MHz	θ	_____	rad	±228 mrad	_____	mrad	±2 mrad
10 MHz	|Z|	_____	kΩ	±70.3 Ω	_____	Ω	±4.4 Ω
10 MHz	θ	_____	rad	±32.2 mrad	_____	mrad	±2.0 mrad
100 MHz	|Z|	_____	Ω	±2.86 Ω	_____	Ω	±0.43 Ω
100 MHz	θ	_____	rad	±13.4 mrad	_____	mrad	±2.0 mrad
200 MHz	|Z|	_____	Ω	±1.62 Ω	_____	Ω	±0.25 Ω
200 MHz	θ	_____	rad	±16.0 mrad	_____	mrad	±2.5 mrad
300 MHz	|Z|	_____	Ω	±1.15 Ω	_____	mΩ	±0.18 Ω
300 MHz	θ	_____	rad	±18.8 mrad	_____	mrad	±3.0 mrad
500 MHz	|Z|	_____	Ω	±836 mΩ	_____	mΩ	±90 mΩ
500 MHz	θ	_____	rad	±37.1 mrad	_____	mrad	±4.0 mrad
600 MHz	|Z|	_____	Ω	±860 mΩ	_____	mΩ	±88 mΩ
600 MHz	θ	_____	rad	±87.6 mrad	_____	mrad	±9.0 mrad
800 MHz	|Z|	_____	Ω	±1.14 Ω	_____	mΩ	±0.12 Ω
800 MHz	θ	_____	rad	±83.5 mrad	_____	mrad	±9.0 mrad
1 GHz	|Z|	_____	Ω	±2.17 Ω	_____	Ω	±0.27 Ω
1 GHz	θ	_____	rad	±49.2 mrad	_____	mrad	±6.0 mrad
1.6 GHz	|Z|	_____	Ω	±6.70 Ω	_____	Ω	±0.86 Ω
1.6 GHz	θ	_____	rad	±78.1 mrad	_____	mrad	±10.0 mrad
1.8 GHz	|Z|	_____	Ω	±3.30 Ω	_____	Ω	±0.33 Ω
1.8 GHz	θ	_____	rad	±99.7 mrad	_____	mrad	±10.0 mrad

Test Head: High-Temp High-Z
Standard: 10 cm Airline with Open
Osc Level: 41 mV

Frequency	Measurement Parameter	Calibration Value		Test Limit	Test Result		Measurement Uncertainty
1 MHz	|Z|	_____	kΩ	±9.74 kΩ	_____	kΩ	±0.04 kΩ
1 MHz	θ	_____	rad	±447 mrad	_____	mrad	±2 mrad
10 MHz	|Z|	_____	kΩ	±118 Ω	_____	Ω	±4 Ω
10 MHz	θ	_____	rad	±54.0 mrad	_____	mrad	±2.0 mrad
100 MHz	|Z|	_____	Ω	±3.32 Ω	_____	Ω	±0.43 Ω
100 MHz	θ	_____	rad	±15.5 mrad	_____	mrad	±2.0 mrad
200 MHz	|Z|	_____	Ω	±1.73 Ω	_____	Ω	±0.25 Ω
200 MHz	θ	_____	rad	±17.0 mrad	_____	mrad	±2.5 mrad
300 MHz	|Z|	_____	Ω	±1.18 Ω	_____	mΩ	±0.18 mΩ
300 MHz	θ	_____	rad	±19.4 mrad	_____	mrad	±3.0 mrad
500 MHz	|Z|	_____	Ω	±841 mΩ	_____	mΩ	±90 mΩ
500 MHz	θ	_____	rad	±37.3 mrad	_____	mrad	±4.0 mrad
600 MHz	|Z|	_____	Ω	±861 mΩ	_____	mΩ	±88 mΩ
600 MHz	θ	_____	rad	±87.7 mrad	_____	mrad	±9.0 mrad
800 MHz	|Z|	_____	Ω	±1.14 Ω	_____	mΩ	±0.12 Ω
800 MHz	θ	_____	rad	±83.7 mrad	_____	mrad	±9.0 mrad
1 GHz	|Z|	_____	Ω	±2.19 Ω	_____	Ω	±0.27 Ω
1 GHz	θ	_____	rad	±49.6 mrad	_____	mrad	±6.0 mrad
1.6 GHz	|Z|	_____	Ω	±6.77 Ω	_____	Ω	±0.86 Ω
1.6 GHz	θ	_____	rad	±79.0 mrad	_____	mrad	±10.0 mrad
1.8 GHz	|Z|	_____	Ω	±3.31 Ω	_____	Ω	±0.33 Ω
1.8 GHz	θ	_____	rad	±100 mrad	_____	mrad	±10 mrad

Test Head: High-Temp High-Z
Standard: 10 cm Airline with Short
Osc Level: 250 mV

Frequency	Measurement Parameter	Calibration Value		Test Limit	Test Result		Measurement Uncertainty
1 MHz	|Z|	_____	mΩ	±102 mΩ	_____	mΩ	±2 mΩ
1 MHz	θ	_____	rad	±897 mrad	_____	mrad	±15 mrad
10 MHz	|Z|	_____	Ω	±116 mΩ	_____	mΩ	±4 mΩ
10 MHz	θ	_____	rad	±109 mrad	_____	mrad	±4 mrad
100 MHz	|Z|	_____	Ω	±268 mΩ	_____	mΩ	±27 mΩ
100 MHz	θ	_____	rad	±25.0 mrad	_____	mrad	±2.5 mrad
200 MHz	|Z|	_____	Ω	±504 mΩ	_____	mΩ	±67 mΩ
200 MHz	θ	_____	rad	±22.5 mrad	_____	mrad	±3.0 mrad
300 MHz	|Z|	_____	Ω	±786 mΩ	_____	mΩ	±110 mΩ
300 MHz	θ	_____	rad	±21.5 mrad	_____	mrad	±3.0 mrad
500 MHz	|Z|	_____	Ω	±2.13 Ω	_____	Ω	±0.31 Ω
500 MHz	θ	_____	rad	±24.5 mrad	_____	mrad	±3.5 mrad
600 MHz	|Z|	_____	Ω	±6.16 Ω	_____	Ω	±0.78 Ω
600 MHz	θ	_____	rad	±39.7 mrad	_____	mrad	±5.0 mrad
1 GHz	|Z|	_____	Ω	±3.95 Ω	_____	Ω	±0.52 Ω
1 GHz	θ	_____	rad	±45.9 mrad	_____	mrad	±6.0 mrad
1.3 GHz	|Z|	_____	Ω	±2.19 Ω	_____	Ω	±0.22 Ω
1.3 GHz	θ	_____	rad	±99.4 mrad	_____	mrad	±10.0 mrad
1.6 GHz	|Z|	_____	Ω	±2.06 Ω	_____	Ω	±0.16 Ω
1.6 GHz	θ	_____	rad	±191 mrad	_____	mrad	±15 mrad
1.8 GHz	|Z|	_____	Ω	±3.50 Ω	_____	Ω	±0.37 Ω
1.8 GHz	θ	_____	rad	±95.4 mrad	_____	mrad	±10.0 mrad

Test Head: High-Temp High-Z
Standard: 10 cm Airline with Short
Osc Level: 41 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	_____ mΩ	±102 mΩ	_____ mΩ	±2 mΩ
1 MHz	θ	_____ rad	±897 mrad	_____ rad	±15 mrad
10 MHz	|Z|	_____ Ω	±116 mΩ	_____ mΩ	±4 mΩ
10 MHz	θ	_____ rad	±109 mrad	_____ mrad	±4 mrad
100 MHz	|Z|	_____ Ω	±269 mΩ	_____ mΩ	±27 mΩ
100 MHz	θ	_____ rad	±25.1 mrad	_____ mrad	±2.5 mrad
200 MHz	|Z|	_____ Ω	±509 mΩ	_____ mΩ	±67 mΩ
200 MHz	θ	_____ rad	±22.7 mrad	_____ mrad	±3.0 mrad
300 MHz	|Z|	_____ Ω	±799 mΩ	_____ mΩ	±110 mΩ
300 MHz	θ	_____ rad	±21.9 mrad	_____ mrad	±3.0 mrad
500 MHz	|Z|	_____ Ω	±2.21 Ω	_____ Ω	±0.31 Ω
500 MHz	θ	_____ rad	±25.3 mrad	_____ mrad	±3.5 mrad
600 MHz	|Z|	_____ Ω	±6.41 Ω	_____ Ω	±0.78 Ω
600 MHz	θ	_____ rad	±41.2 mrad	_____ mrad	±5.0 mrad
1 GHz	|Z|	_____ Ω	±4.02 Ω	_____ Ω	±0.52 Ω
1 GHz	θ	_____ rad	±46.7 mrad	_____ mrad	±6.0 mrad
1.3 GHz	|Z|	_____ Ω	±2.20 Ω	_____ Ω	±0.22 Ω
1.3 GHz	θ	_____ rad	±99.6 mrad	_____ mrad	±10.0 mrad
1.6 GHz	|Z|	_____ Ω	±2.06 Ω	_____ Ω	±0.16 Ω
1.6 GHz	θ	_____ rad	±191 mrad	_____ mrad	±15 mrad
1.8 GHz	|Z|	_____ Ω	±3.51 Ω	_____ Ω	±0.37 Ω
1.8 GHz	θ	_____ rad	±95.8mrad	_____ mrad	±10.0 mrad

High-Temp Low-Impedance Test Head (Option 014)

Test Head: High-Temp Low-Z
Standard: Open
Osc Level: 250 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Y|	_____ μS	±30.2 μS	_____ μS	±0.0 μS
10 MHz	|Y|	_____ μS	±32.2 μS	_____ μS	±0.3 μS
100 MHz	|Y|	_____ μS	±52.4 μS	_____ μS	±3.4 μS
200 MHz	|Y|	_____ μS	±76.4 μS	_____ μS	±6.7 μS
300 MHz	|Y|	_____ mS	±99.9 μS	_____ μS	±10.0 μS
500 MHz	|Y|	_____ mS	±148 μS	_____ μS	±17 μS
600 MHz	|Y|	_____ mS	±189 μS	_____ μS	±21 μS
800 MHz	|Y|	_____ mS	±245 μS	_____ μS	±28 μS
1 GHz	|Y|	_____ mS	±305 μS	_____ μS	±35 μS
1.3 GHz	|Y|	_____ mS	±478 μS	_____ μS	±46 μS
1.6 GHz	|Y|	_____ mS	±604 μS	_____ μS	±63 μS
1.8 GHz	|Y|	_____ mS	±695 μS	_____ μS	±71 μS

Test Head: High-Temp Low-Z
Standard: Open
Osc Level: 41 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Y|	_____ μS	±30.2 μS	_____ μS	±0.0 μS
10 MHz	|Y|	_____ μS	±32.2 μS	_____ μS	±0.3 μS
100 MHz	|Y|	_____ μS	±52.4 μS	_____ μS	±3.4 μS
200 MHz	|Y|	_____ μS	±76.5 μS	_____ μS	±6.7 μS
300 MHz	|Y|	_____ mS	±99.9 μS	_____ μS	±10.0 μS
500 MHz	|Y|	_____ mS	±148 μS	_____ μS	±17 μS
600 MHz	|Y|	_____ mS	±189 μS	_____ μS	±21 μS
800 MHz	|Y|	_____ mS	±246 μS	_____ μS	±28 μS
1 GHz	|Y|	_____ mS	±305 μS	_____ μS	±35 μS
1.3 GHz	|Y|	_____ mS	±479 μS	_____ μS	±46 μS
1.6 GHz	|Y|	_____ mS	±604 μS	_____ μS	±63 μS
1.8 GHz	|Y|	_____ mS	±696 μS	_____ μS	±71 μS

Test Head: High-Temp Low-Z
Standard: Short
Osc Level: 250 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	0.00 mΩ	±31.0 mΩ	_____ mΩ	±1.8 mΩ
10 MHz	|Z|	0.00 mΩ	±40.0 mΩ	_____ mΩ	±2.0 mΩ
100 MHz	|Z|	0.00 mΩ	±130 mΩ	_____ mΩ	±10 mΩ
200 MHz	|Z|	0.00 mΩ	±230 mΩ	_____ mΩ	±20 mΩ
300 MHz	|Z|	0.00 mΩ	±330 mΩ	_____ mΩ	±30 mΩ
500 MHz	|Z|	0.00 mΩ	±530 mΩ	_____ mΩ	±40 mΩ
600 MHz	|Z|	0.00 mΩ	±630 mΩ	_____ mΩ	±50 mΩ
800 MHz	|Z|	0.00 mΩ	±830 mΩ	_____ mΩ	±70 mΩ
1 GHz	|Z|	0.00 mΩ	±1.03 Ω	_____ mΩ	±0.08 Ω
1.3 GHz	|Z|	0.00 mΩ	±1.33 Ω	_____ mΩ	±0.10 Ω
1.6 GHz	|Z|	0.00 mΩ	±1.63 Ω	_____ mΩ	±0.12 Ω
1.8 GHz	|Z|	0.00 mΩ	±1.83 Ω	_____ mΩ	±0.13 Ω

Test Head: High-Temp Low-Z
Standard: Short
Osc Level: 41 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	0.00 mΩ	±51.0 mΩ	_____ mΩ	±1.8 mΩ
10 MHz	|Z|	0.00 mΩ	±60.0 mΩ	_____ mΩ	±2.0 mΩ
100 MHz	|Z|	0.00 mΩ	±150 mΩ	_____ mΩ	±10 mΩ
200 MHz	|Z|	0.00 mΩ	±250 mΩ	_____ mΩ	±20 mΩ
300 MHz	|Z|	0.00 mΩ	±350 mΩ	_____ mΩ	±30 mΩ
500 MHz	|Z|	0.00 mΩ	±550 mΩ	_____ mΩ	±40 mΩ
600 MHz	|Z|	0.00 mΩ	±650 mΩ	_____ mΩ	±50 mΩ
800 MHz	|Z|	0.00 mΩ	±850 mΩ	_____ mΩ	±70 mΩ
1 GHz	|Z|	0.00 mΩ	±1.05 Ω	_____ mΩ	±0.08 Ω
1.3 GHz	|Z|	0.00 mΩ	±1.35 Ω	_____ mΩ	±0.10 Ω
1.6 GHz	|Z|	0.00 mΩ	±1.65 Ω	_____ mΩ	±0.12 Ω
1.8 GHz	|Z|	0.00 mΩ	±1.85 Ω	_____ mΩ	±0.13 Ω

Test Head: High-Temp Low-Z
Standard: 50 Ω
Osc Level: 250 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	_____ Ω	±407 mΩ	_____ mΩ	±90 mΩ
1 MHz	θ	_____ mrad	±8.13 mrad	_____ mrad	±1.80 mrad
10 MHz	|Z|	_____ Ω	±420 mΩ	_____ mΩ	±90 mΩ
10 MHz	θ	_____ mrad	±8.40 mrad	_____ mrad	±1.80 mrad
100 MHz	|Z|	_____ Ω	±555 mΩ	_____ mΩ	±100 mΩ
100 MHz	θ	_____ mrad	±11.1 mrad	_____ mrad	±2.0 mrad
200 MHz	|Z|	_____ Ω	±805 mΩ	_____ mΩ	±125 mΩ
200 MHz	θ	_____ mrad	±16.1 mrad	_____ mrad	±2.5 mrad
300 MHz	|Z|	_____ Ω	±955 mΩ	_____ mΩ	±150 mΩ
300 MHz	θ	_____ mrad	±19.1 mrad	_____ mrad	±3.0 mrad
500 MHz	|Z|	_____ Ω	±1.26 Ω	_____ mΩ	±0.20 Ω
500 MHz	θ	_____ mrad	±25.1 mrad	_____ mrad	±4.0 mrad
600 MHz	|Z|	_____ Ω	±1.76 Ω	_____ Ω	±0.25 Ω
600 MHz	θ	_____ mrad	±35.1 mrad	_____ mrad	±5.0 mrad
800 MHz	|Z|	_____ Ω	±2.06 Ω	_____ Ω	±0.25 Ω
800 MHz	θ	_____ mrad	±41.1 mrad	_____ mrad	±5.0 mrad
1 GHz	|Z|	_____ Ω	±2.36 Ω	_____ Ω	±0.25 Ω
1 GHz	θ	_____ mrad	±47.1 mrad	_____ mrad	±5.0 mrad
1.3 GHz	|Z|	_____ Ω	±3.56 Ω	_____ Ω	±0.25 Ω
1.3 GHz	θ	_____ mrad	±71.1 mrad	_____ mrad	±5.0 mrad
1.6 GHz	|Z|	_____ Ω	±4.01 Ω	_____ Ω	±0.25 Ω
1.6 GHz	θ	_____ mrad	±80.1 mrad	_____ mrad	±5.0 mrad
1.8 GHz	|Z|	_____ Ω	±4.31 Ω	_____ Ω	±0.25 Ω
1.8 GHz	θ	_____ mrad	±86.1 mrad	_____ mrad	±5.0 mrad

Test Head: High-Temp Low-Z
Standard: 50 Ω
Osc Level: 41 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	_____ Ω	±427 mΩ	_____ mΩ	±90 mΩ
1 MHz	θ	_____ mrad	±8.53 mrad	_____ mrad	±1.80 mrad
10 MHz	|Z|	_____ Ω	±440 mΩ	_____ mΩ	±90 mΩ
10 MHz	θ	_____ mrad	±8.80 mrad	_____ mrad	±1.80 mrad
100 MHz	|Z|	_____ Ω	±575 mΩ	_____ mΩ	±100 mΩ
100 MHz	θ	_____ mrad	±11.5 mrad	_____ mrad	±2.0 mrad
200 MHz	|Z|	_____ Ω	±825 mΩ	_____ mΩ	±125 mΩ
200 MHz	θ	_____ mrad	±16.5 mrad	_____ mrad	±2.5 mrad
300 MHz	|Z|	_____ Ω	±975 mΩ	_____ mΩ	±150 mΩ
300 MHz	θ	_____ mrad	±19.5 mrad	_____ mrad	±3.0 mrad
500 MHz	|Z|	_____ Ω	±1.28 Ω	_____ mΩ	±0.20 Ω
500 MHz	θ	_____ mrad	±25.5 mrad	_____ mrad	±4.0 mrad
600 MHz	|Z|	_____ Ω	±1.78 Ω	_____ Ω	±0.25 Ω
600 MHz	θ	_____ mrad	±35.5 mrad	_____ mrad	±5.0 mrad
800 MHz	|Z|	_____ Ω	±2.08 Ω	_____ Ω	±0.25 Ω
800 MHz	θ	_____ mrad	±41.5 mrad	_____ mrad	±5.0 mrad
1 GHz	|Z|	_____ Ω	±2.38 Ω	_____ Ω	±0.25 Ω
1 GHz	θ	_____ mrad	±47.5 mrad	_____ mrad	±5.0 mrad
1.3 GHz	|Z|	_____ Ω	±3.58 Ω	_____ Ω	±0.25 Ω
1.3 GHz	θ	_____ mrad	±71.5 mrad	_____ mrad	±5.0 mrad
1.6 GHz	|Z|	_____ Ω	±4.03 Ω	_____ Ω	±0.25 Ω
1.6 GHz	θ	_____ mrad	±80.5 mrad	_____ mrad	±5.0 mrad
1.8 GHz	|Z|	_____ Ω	±4.33 Ω	_____ Ω	±0.25 Ω
1.8 GHz	θ	_____ mrad	±86.5 mrad	_____ mrad	±5.0 mrad

Test Head: High-Temp Low-Z
Standard: 10 cm Airline with Open
Osc Level: 250 mV

Frequency	Measurement Parameter	Calibration Value		Test Limit	Test Result		Measurement Uncertainty
1 MHz	|Z|	_____	kΩ	±14.5 kΩ	_____	kΩ	±0.0 kΩ
1 MHz	θ	_____	rad	±665 mrad	_____	mrad	±2 mrad
10 MHz	|Z|	_____	kΩ	±165 Ω	_____	Ω	±4 Ω
10 MHz	θ	_____	rad	±75.8 mrad	_____	mrad	±2.0 mrad
100 MHz	|Z|	_____	Ω	±3.71 Ω	_____	Ω	±0.43 Ω
100 MHz	θ	_____	rad	±17.3 mrad	_____	mrad	±2.0 mrad
200 MHz	|Z|	_____	Ω	±1.76 Ω	_____	Ω	±0.25 Ω
200 MHz	θ	_____	rad	±17.4 mrad	_____	mrad	±2.5 mrad
300 MHz	|Z|	_____	Ω	±1.15 Ω	_____	mΩ	±0.18 Ω
300 MHz	θ	_____	rad	±18.9 mrad	_____	mrad	±3.0 mrad
500 MHz	|Z|	_____	Ω	±776 mΩ	_____	mΩ	±90 mΩ
500 MHz	θ	_____	rad	±34.4 mrad	_____	mrad	±4.0 mrad
600 MHz	|Z|	_____	Ω	±792 mΩ	_____	mΩ	±88 mΩ
600 MHz	θ	_____	rad	±80.7 mrad	_____	mrad	±9.0 mrad
800 MHz	|Z|	_____	Ω	±1.07 Ω	_____	mΩ	±0.12 Ω
800 MHz	θ	_____	rad	±78.7 mrad	_____	mrad	±9.0 mrad
1 GHz	|Z|	_____	Ω	±2.14 Ω	_____	Ω	±0.27 Ω
1 GHz	θ	_____	rad	±48.5 mrad	_____	mrad	±6.0 mrad
1.6 GHz	|Z|	_____	Ω	±6.77 Ω	_____	Ω	±0.86 Ω
1.6 GHz	θ	_____	rad	±79.0 mrad	_____	mrad	±10.0 mrad
1.8 GHz	|Z|	_____	Ω	±3.25 Ω	_____	Ω	±0.33 Ω
1.8 GHz	θ	_____	rad	±98.2 mrad	_____	mrad	±10.0 mrad

Test Head: High-Temp Low-Z
Standard: 10 cm Airline with Open
Osc Level: 41 mV

Frequency	Measurement Parameter	Calibration Value		Test Limit	Test Result		Measurement Uncertainty
1 MHz	|Z|	_____	kΩ	±14.5 kΩ	_____	kΩ	±0.0 kΩ
1 MHz	θ	_____	rad	±665 mrad	_____	mrad	±2 mrad
10 MHz	|Z|	_____	kΩ	±165 Ω	_____	Ω	±4 Ω
10 MHz	θ	_____	rad	±75.8 mrad	_____	mrad	±2.0 mrad
100 MHz	|Z|	_____	Ω	±3.73 Ω	_____	Ω	±0.43 Ω
100 MHz	θ	_____	rad	±17.4 mrad	_____	mrad	±2.0 mrad
200 MHz	|Z|	_____	Ω	±1.78 Ω	_____	Ω	±0.25 Ω
200 MHz	θ	_____	rad	±17.6 mrad	_____	mrad	±2.5 mrad
300 MHz	|Z|	_____	Ω	±1.17 Ω	_____	mΩ	±0.18 Ω
300 MHz	θ	_____	rad	±19.2 mrad	_____	mrad	±3.0 mrad
500 MHz	|Z|	_____	Ω	±796 mΩ	_____	mΩ	±90 mΩ
500 MHz	θ	_____	rad	±35.3 mrad	_____	mrad	±4.0 mrad
600 MHz	|Z|	_____	Ω	±812 mΩ	_____	mΩ	±88 mΩ
600 MHz	θ	_____	rad	±82.7 mrad	_____	mrad	±9.0 mrad
800 MHz	|Z|	_____	Ω	±1.09 Ω	_____	mΩ	±122 mΩ
800 MHz	θ	_____	rad	±80.1 mrad	_____	mrad	±9.0 mrad
1 GHz	|Z|	_____	Ω	±2.16 Ω	_____	Ω	±0.27 Ω
1 GHz	θ	_____	rad	±48.9 mrad	_____	mrad	±6.0 mrad
1.6 GHz	|Z|	_____	Ω	±6.79 Ω	_____	Ω	±0.86 Ω
1.6 GHz	θ	_____	rad	±79.3 mrad	_____	mrad	±10.0 mrad
1.8 GHz	|Z|	_____	Ω	±3.27 Ω	_____	Ω	±0.33 Ω
1.8 GHz	θ	_____	rad	±98.9 mrad	_____	mrad	±10.0 mrad

Test Head: High-Temp Low-Z
Standard: 10 cm Airline with Short
Osc Level: 250 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	_____ mΩ	±31.7 mΩ	_____ mΩ	±1.7 mΩ
1 MHz	θ	_____ rad	±280 mrad	_____ mrad	±15 mrad
10 MHz	|Z|	_____ Ω	±46.5 mΩ	_____ mΩ	±4.3 mΩ
10 MHz	θ	_____ rad	±43.3 mrad	_____ mrad	±4.0 mrad
100 MHz	|Z|	_____ Ω	±200 mΩ	_____ mΩ	±27 mΩ
100 MHz	θ	_____ rad	±18.7 mrad	_____ mrad	±2.5 mrad
200 MHz	|Z|	_____ Ω	±444 mΩ	_____ mΩ	±67 mΩ
200 MHz	θ	_____ rad	±19.8 mrad	_____ mrad	±3.0 mrad
300 MHz	|Z|	_____ Ω	±742 mΩ	_____ mΩ	±110 mΩ
300 MHz	θ	_____ rad	±20.3 mrad	_____ mrad	±3.0 mrad
500 MHz	|Z|	_____ Ω	±2.22 Ω	_____ Ω	±0.31 Ω
500 MHz	θ	_____ rad	±25.4 mrad	_____ mrad	±3.5 mrad
600 MHz	|Z|	_____ Ω	±6.58 Ω	_____ Ω	±0.78 Ω
600 MHz	θ	_____ rad	±42.4 mrad	_____ mrad	±5.0 mrad
1 GHz	|Z|	_____ Ω	±4.03 Ω	_____ Ω	±0.52 Ω
1 GHz	θ	_____ rad	±46.8 mrad	_____ mrad	±6.0 mrad
1.3 GHz	|Z|	_____ Ω	±2.13 Ω	_____ Ω	±0.22 Ω
1.3 GHz	θ	_____ rad	±96.6 mrad	_____ mrad	±10.0 mrad
1.6 GHz	|Z|	_____ Ω	±2.00 Ω	_____ Ω	±0.16 Ω
1.6 GHz	θ	_____ rad	±184 mrad	_____ mrad	±15 mrad
1.8 GHz	|Z|	_____ Ω	±3.45 Ω	_____ Ω	±0.37 Ω
1.8 GHz	θ	_____ rad	±94.2 mrad	_____ mrad	±10.0 mrad

Test Head: High-Temp Low-Z
Standard: 10 cm Airline with Short
Osc Level: 41 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	_____ mΩ	±51.7 mΩ	_____ mΩ	±1.7 mΩ
1 MHz	θ	_____ rad	±456 mrad	_____ mrad	±15 mrad
10 MHz	|Z|	_____ Ω	±66.5 mΩ	_____ mΩ	±4.3 mΩ
10 MHz	θ	_____ rad	±62.0 mrad	_____ mrad	±4.0 mrad
100 MHz	|Z|	_____ Ω	±220 mΩ	_____ mΩ	±27 mΩ
100 MHz	θ	_____ rad	±20.5 mrad	_____ mrad	±2.5 mrad
200 MHz	|Z|	_____ Ω	±464 mΩ	_____ mΩ	±67 mΩ
200 MHz	θ	_____ rad	±20.7 mrad	_____ mrad	±3.0 mrad
300 MHz	|Z|	_____ Ω	±762 mΩ	_____ mΩ	±110 mΩ
300 MHz	θ	_____ rad	±20.9 mrad	_____ mrad	±3.0 mrad
500 MHz	|Z|	_____ Ω	±2.24 Ω	_____ Ω	±0.31 Ω
500 MHz	θ	_____ rad	±25.6 mrad	_____ mrad	±3.5 mrad
600 MHz	|Z|	_____ Ω	±6.60 Ω	_____ Ω	±0.78 Ω
600 MHz	θ	_____ rad	±42.5 mrad	_____ mrad	±5.0 mrad
1 GHz	|Z|	_____ Ω	±4.05 Ω	_____ Ω	±0.52 Ω
1 GHz	θ	_____ rad	±47.0 mrad	_____ mrad	±6.0 mrad
1.3 GHz	|Z|	_____ Ω	±2.15 Ω	_____ Ω	±0.22 Ω
1.3 GHz	θ	_____ rad	±97.5 mrad	_____ mrad	±10.0 mrad
1.6 GHz	|Z|	_____ Ω	±2.02 Ω	_____ Ω	±0.16 Ω
1.6 GHz	θ	_____ rad	±186 mrad	_____ mrad	±15 mrad
1.8 GHz	|Z|	_____ Ω	±3.47 Ω	_____ Ω	±0.37 Ω
1.8 GHz	θ	_____ rad	±94.8 mrad	_____ mrad	±10.0 mrad

DC Bias Accuracy Test

Bias Level	Test Limit	Test Result	Measurement Uncertainty
0 V	±4.00 mV	_____ mV	±0.02 mV
4 V	±8.00 mV	_____ mV	±0.07 mV
10 V	±14.0 mV	_____ mV	±0.1 mV
40 V	±44.0 mV	_____ mV	±1.1 mV
−4 V	±8.00 mV	_____ mV	±0.07 mV
−10 V	±14.0 mV	_____ mV	±0.1 mV
−40 V	±44.0 mV	_____ mV	±1.1 mV
0 A	±30.0 μA	_____ μA	±0.0 μA
20 μA	±30.1 μA	_____ μA	±0.0 μA
1 mA	±35.0 μA	_____ μA	±0.1 μA
10 mA	±80.0 μA	_____ μA	±0.9 μA
100 mA	±530 μA	_____ μA	±18 μA
−20 μA	±30.1 μA	_____ μA	±0.0 μA
−1 mA	±35.0 μA	_____ μA	±0.1 μA
−10 mA	±80.0 μA	_____ μA	±0.9 μA
−100 mA	±530 μA	_____ μA	±18 μA

3

Adjustments and Correction Constants

INTRODUCTION

This chapter describes the Adjustments and Correction Constants procedures required to ensure that the HP 4291B RF Impedance/Material Analyzer is within its specifications. These adjustments should be performed along with periodic maintenance to keep the analyzer in optimum operating condition. The recommended calibration period is 12 months. If proper performance cannot be achieved after the Adjustments and Correction Constants procedures are performed, see Chapter 4.

Note

The correction constants are empirically derived data that is stored in memory and then recalled to refine the analyzer's measurement and to define its operation.

SAFETY CONSIDERATIONS

This manual contains NOTEs, CAUTIONs, and WARNINGs that must be followed to ensure the safety of the operator and to keep the instrument in a safe and serviceable condition. The adjustments must be performed by qualified service personnel.

Warning

Any interruption of the protective ground conductor (inside or outside the analyzer) or disconnection of the protective ground terminal can make the instrument dangerous. Intentional interruption of the protective ground system for any reason is prohibited.

The removal or opening of covers for adjustment, or removal of parts other than those that are accessible by hand will expose circuits containing dangerous voltage levels.

Remember that the capacitors in the analyzer can remain charged for several minutes, even through you have turned the analyzer OFF and unplugged it.

Warning

The adjustments described in this chapter are performed with power applied and the protective covers removed. Dangerous voltage levels exist at many points and can result in serious personal injury or death if you come into contact with them.

REQUIRED EQUIPMENT

Table 1-1 lists the equipment required to perform the Adjustments and the Correction Constants procedures described in this chapter. Use only calibrated test equipment when adjusting the analyzer. If the recommended test equipment is not available, equipment whose specifications are equal to, or surpasses those of the recommended test equipment may be used.

WARM-UP FOR ADJUSTMENTS AND CORRECTION CONSTANTS

Warm-up the analyzer for at least 30 minute before performing any of the following Adjustments and Correction Constants procedures to ensure proper results and correct instrument operation.

INSTRUMENT COVER REMOVAL

To gain access to the adjustment components, you need to remove the top cover and the side covers. When removing these covers, see Chapter 13.

ORDER OF ADJUSTMENTS

When performing more than one Adjustments or Correction Constants procedure, perform them in the order they appear in this chapter. The procedures are presented in the following order:

- 40 MHz Reference Oscillator Frequency Adjustment
- 520 MHz Level Adjustment
- Comb Generator Adjustment
- Step Pretune Correction Constants
- Second Local PLL Lock Adjustment
- Source VCXO Adjustment
- Third Local VCXO Adjustment
- Source Mixer Local Leakage Adjustment
- OSC Level Correction Constants
- Hold Step Adjustment
- Band Pass Filter Adjustment
- DC Bias Level Correction Constants (Option 001)

UPDATING Correction Constants USING THE ADJUSTMENTS PROGRAM

This section provides general information on how to update the Correction Constants using the adjustments program.

Adjustments Program

The adjustments program is provided on one double-sided diskette. The diskette's HP part number is 04291-65003. The files contained on the diskette are as follows:

ADJ4291B	Adjustments Program
TE_A4291B	Equipment Configuration Program

Note

To prevent accidental deletion or destruction of the program, make working copies of the furnished master diskette (HFS or SRM system). Use the working copies for daily use. Keep the master diskettes in a safe place and use them only for making working copies.

Keyboard and Mouse Operation

The menus in "ADJ4291B" use a window format. The window format menu supports keyboard and mouse operations as follows:

- Keyboard Operation
  1. Press (▲), (▼) keys until your preference is highlighted.
  2. Choose the highlighted item by pressing (RETURN) or (SELECT). (Press (ENTER) or (EXECUTE), if Nimitz Keyboard.)
  3. If `QUIT` or `EXIT` is displayed in a menu, select one of these to exit the menu. Otherwise, press (▶) ((CONTINUE), if Nimitz Keyboard) to exit. When you exit menus, the program displays another menu.

Note

Press (?) to access on-screen help information for the selection you have highlighted. Help information appears in a display window.

Press (RETURN) or (SELECT) (press (ENTER) or (EXECUTE), if Nimitz Keyboard) to turn off the help screen.

- Mouse Operation
  1. Slide the mouse up or down until your preference is highlighted.
  2. Choose the highlighted item by pressing the left-hand button on the mouse, or slide the mouse to the right.
  3. If `QUIT` or `EXIT` is displayed in a menu, select one of these to exit the menu. Otherwise, slide the mouse to the left to exit. When you exit menus, the program displays another menu.

Note

Press the right-hand mouse button to access on-screen help information for the selection you have highlighted. Help information appears in a display window.

Press the left-hand mouse button to turn off the help screen.

Controller Requirement

The following controller system is required to run the adjustments program:

Controller	HP 9000 Series 200/300 computer
	Excluding HP 9826A computers
	Must have inverse video capability
	At least 4 M bytes of RAM
Mass Storage	At least one 3.5 inch HP-IB Flexible Disk Drive
	HFS formatted hard disk system or SRM system are supported.

The controller must be equipped with HP BASIC versions between 5.1 and 5.13, and the language extension files listed in Table 3-1.

Table 3-1. Required Binaries

Name	Version	Description
GRAPH	5.2	Graphics
GRAPHX	5.2	Graphics Extensions
IO	5.1	I/O
MAT	5.1	Matrix Statements
PDEV	5.0	Program Development
KBD	5.1	Keyboard Extensions
CLOCK	5.0	Clock
MS	5.1	Mass Storage
ERR	5.1	Error Message
DISC	5.0	Small Disc Driver
CS80	5.0	CS80 Disc Driver
HPIB	5.0	HP-IB Interface Driver
FHPIB	5.0	HP-IB Interface Driver
CRTB	5.2	Bit-mapped CRT Driver
CRTA	5.1	Alpha CRT Driver
CRTX	5.1	CRT Extensions
EDIT	5.1	List and Edit
SRM	5.1	Shared Resource Management
DCOMM	5.0	Datacomm Interface Driver
HFS	5.3	Hierarchical File System
COMPLEX	5.1	Complex Arithmetic

Updating Correction Constants

Correction Constants are updated using the following procedure:

1. Connect the equipment as shown in Figure 3-1

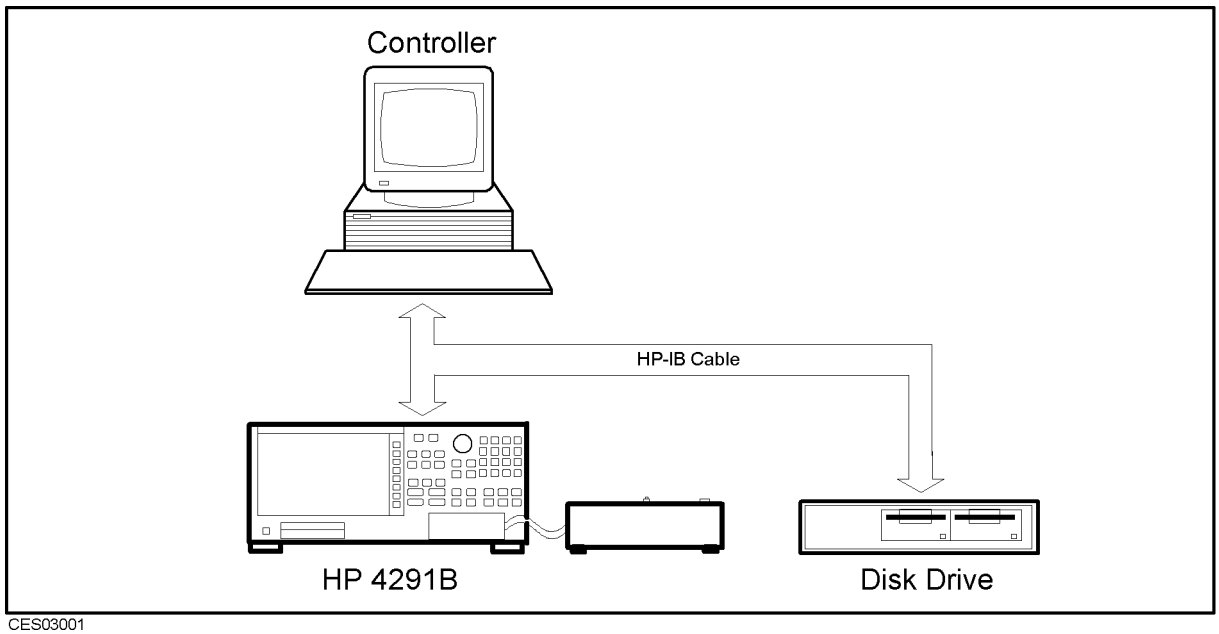


Figure 3-1. Updating Correction Constants Setup

Note

Steps 2 to 5 are used to select the equipment and to set their HP-IB addresses. When you perform the Adjustments Program the first time, perform these steps to select the equipment and the HP-IB address. After that, perform the "TE_A4291B" program only when you want to change the equipment or the HP-IB address.

2. Locate the Equipment Configuration Program "TE_A4291B" in the address of the drive or the directory where the Adjustment Program "ADJ4291B" will be run.
3. Set the mass storage unit specifier (MSUS) to the address of the drive or the directory where "TE_A4291B" is located.
4. Load and run "TE_A4291B".
5. Follow the instructions on the controller's screen until the program ends.
6. Set the mass storage unit specifier (MSUS) to the address of the drive or the directory where the Adjustment Program "ADJ4291B" is located.
7. Load and run "ADJ4291B".
8. A window format menu is displayed.
9. Choose "INITIAL SETUP" if you want to update the Calibrated Value for the power sensor.
10. Choose the item that you want to perform.
11. Follow the instruction on the controller's screen until the program ends. The equipment connections are shown in each Correction Constants procedure in this chapter.

40 MHz REFERENCE OSCILLATOR FREQUENCY ADJUSTMENT

The purpose of this procedure is to adjust the 40 MHz reference oscillator frequency.

Required Equipment

Frequency Counter ..... HP 5343A Option 001
SMB(f)-BNC(f) adapter ..... PN 1250-1236
BNC cable, 61 cm ..... PN 8120-1839

Procedure

1. Connect the equipment as shown in Figure 3-2. The A5 "CAL OUT" connector location is shown in Figure 3-3. Do not connect anything to the rear panel "EXT REF" input connector

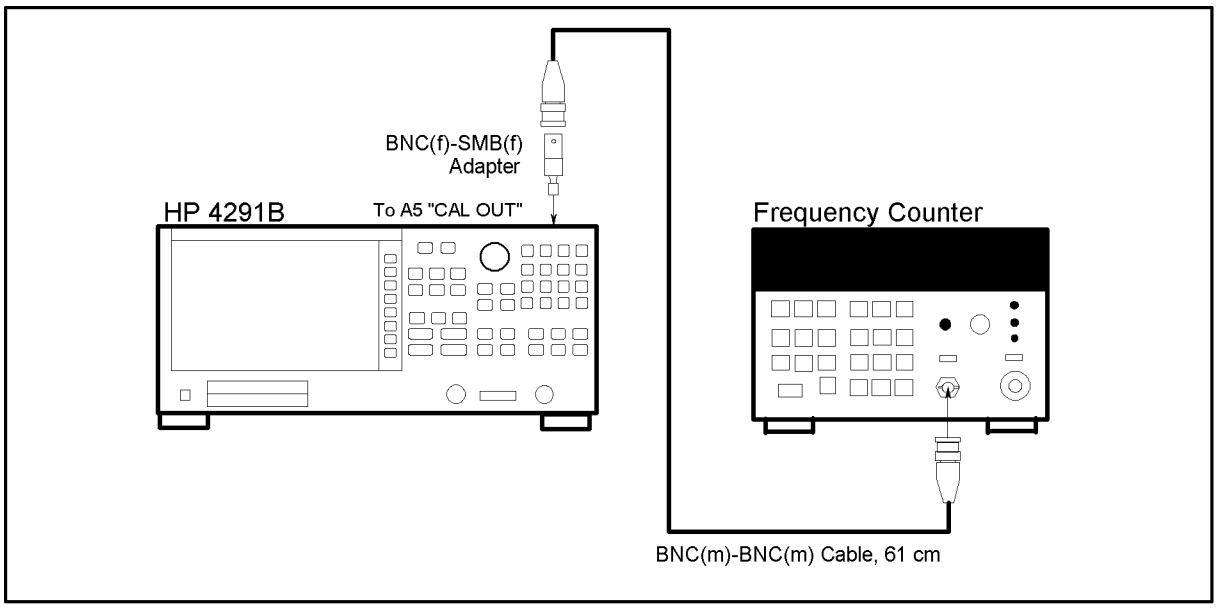
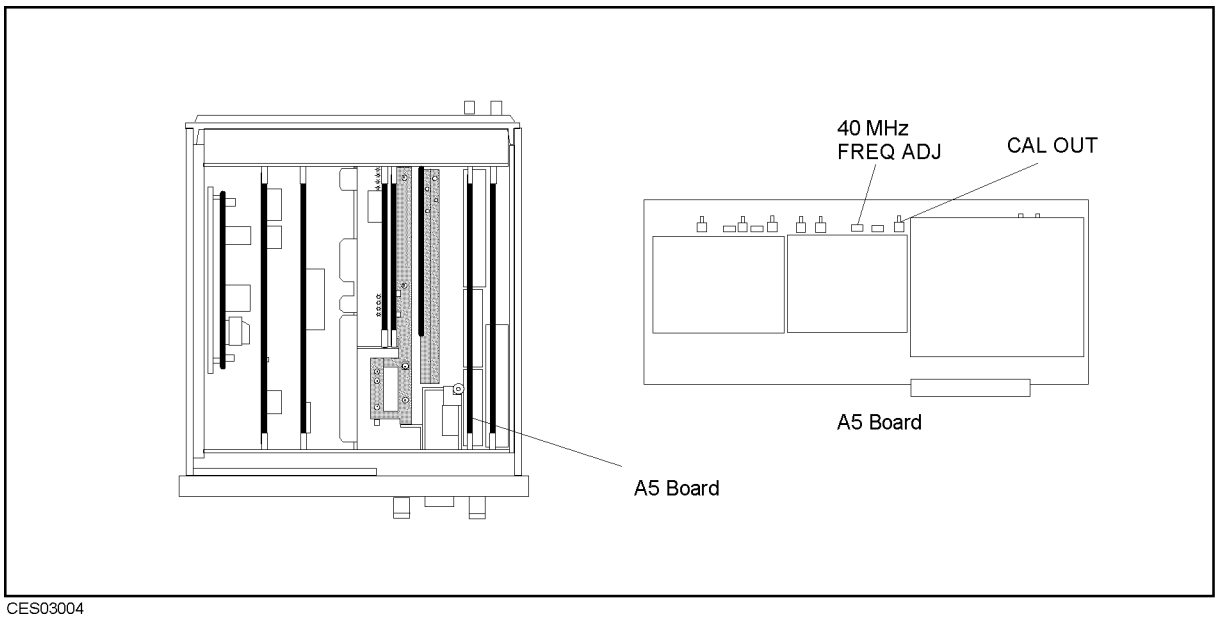


Figure 3-2. 40 MHz Reference Oscillator Frequency Adjustment Setup



CES03004

Figure 3-3. 40 MHz Reference Oscillator Frequency Adjustment Location

2. Set the frequency counter as follows:

   Input Impedance 50 Ω
   Frequency Range 10 Hz - 500 MHz

3. Adjust A5 "40 MHz FREQ ADJ" until the frequency counter reading is within 20 MHz ± 20 Hz. The adjustment location is shown in Figure 3-3.

520 MHz LEVEL ADJUSTMENT

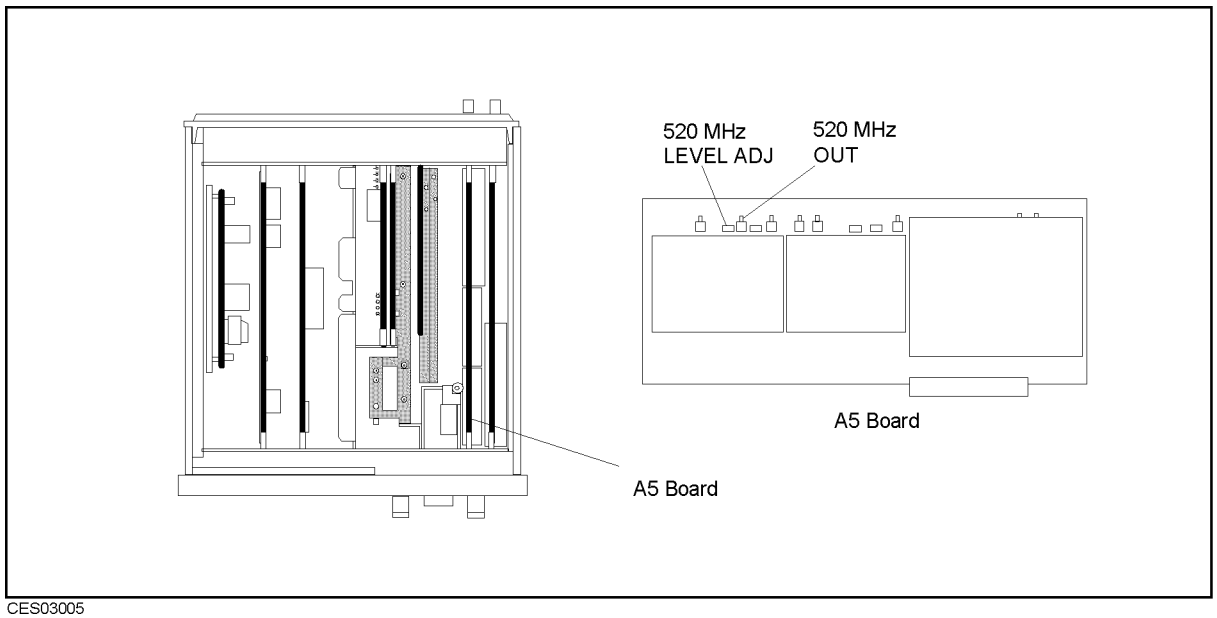
The purpose of this procedure is to adjust the 520 MHz output level.

Required Equipment

Spectrum Analyzer ..... HP 8566A/B
SMC(f)-BNC(f) adapter ..... PN 1250-0832
N(m)-BNC(f) adapter ..... PN 1250-1476
BNC cable, 61 cm ..... PN 8120-1839

Procedure

1. Turn the analyzer OFF.
2. Remove the "J" cable from the A5 "520 MHz OUT" connector. The connector location is shown in Figure 3-4.



CES03005

Figure 3-4. 520 MHz Level Adjustment Location

3. Connect the equipment as shown in Figure 3-5.

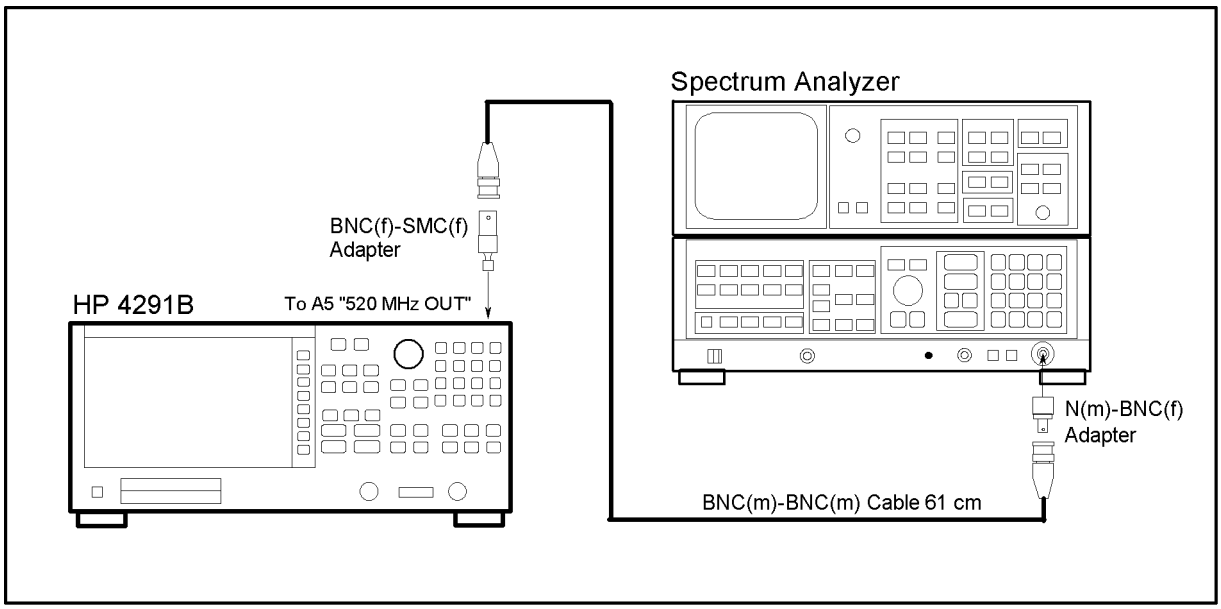


Figure 3-5. 520 MHz Level Adjustment Setup

4. Set the spectrum analyzer as follows:

CENTER Frequency	520 MHz
SPAN	1 MHz
RBW	100 kHz

5. Turn the HP 4291B analyzer ON.
6. Adjust A5 “520 MHz LEVEL ADJ” until the spectrum analyzer reading for the 520 MHz signal level is within -15 ± 0.2 dBm. The adjustment location is shown in Figure 3-4.
7. Turn the HP 4291B analyzer OFF.
8. Reconnect the “J” cable to the A5 “520 MHz OUT” connector.

COMB GENERATOR ADJUSTMENT

The purpose of this procedure is to adjust the comb generator output level.

Required Equipment

Spectrum Analyzer	HP 8566A/B
SMB(f)-BNC(f) adapter	PN 1250-1236
N(m)-BNC(f) adapter	PN 1250-1476
BNC cable, 122 cm	PN 8120-1840

Procedure

1. Turn the HP 4291B analyzer OFF.
2. Remove the SMB connector termination from The A5 "COMB OUT" connector, and connect the equipment as shown in Figure 3-6. The A5 "COMB OUT" connector location is shown in Figure 3-7.

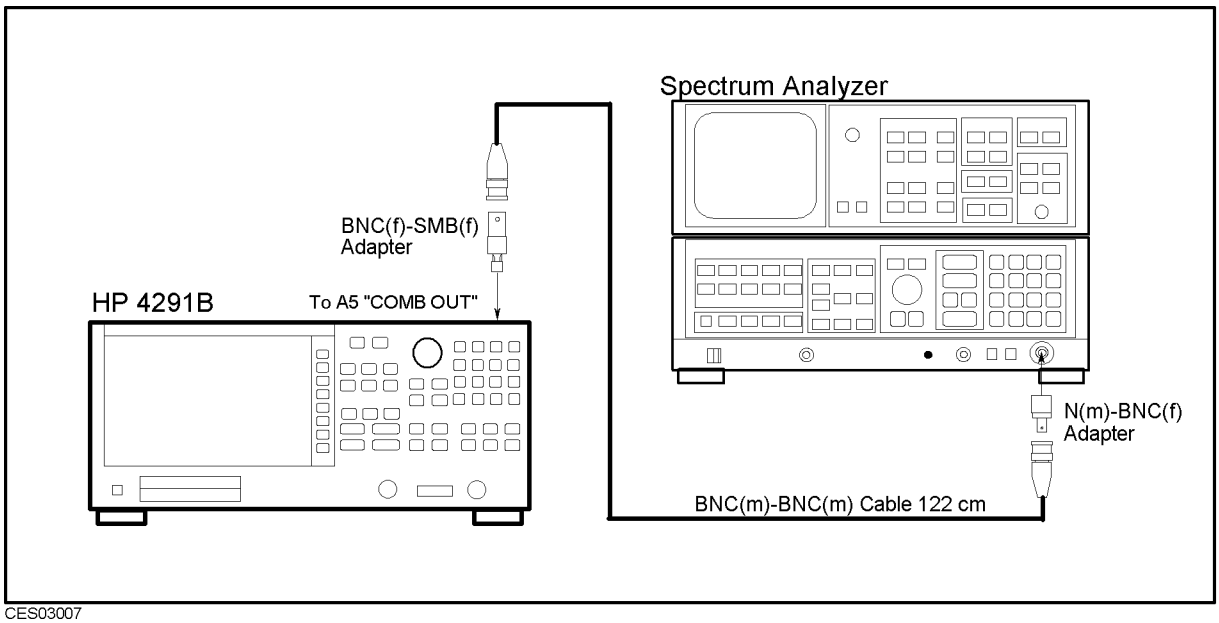
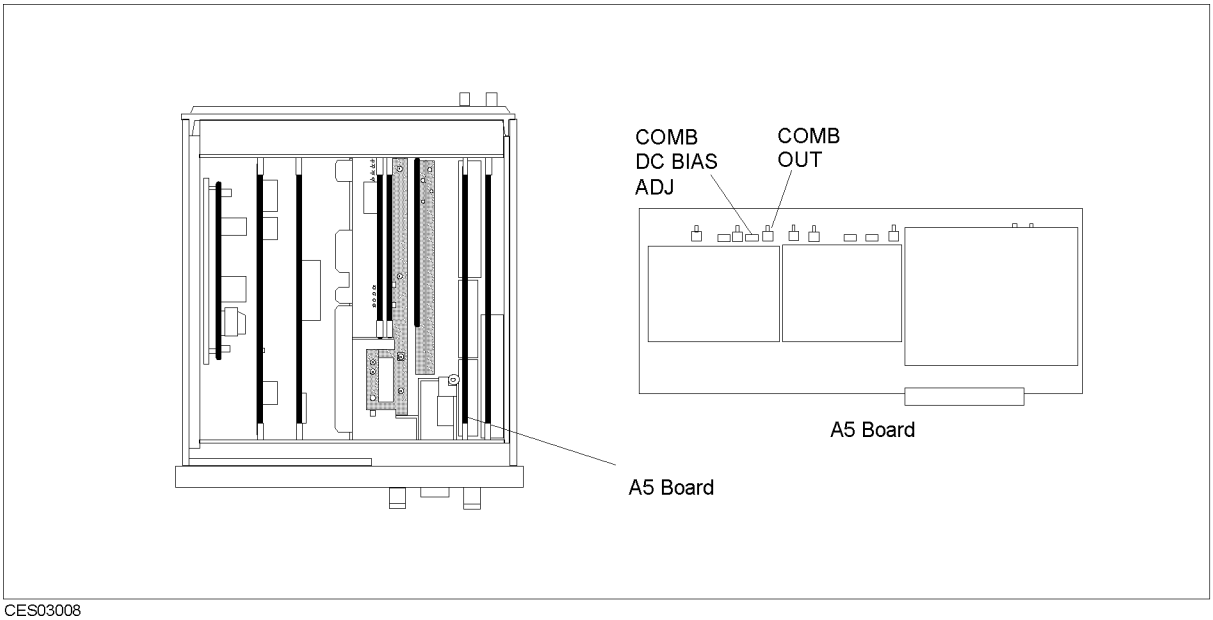


Figure 3-6. Comb Generator Adjustment Setup



CES03008

Figure 3-7. Comb Generator Adjustment Location

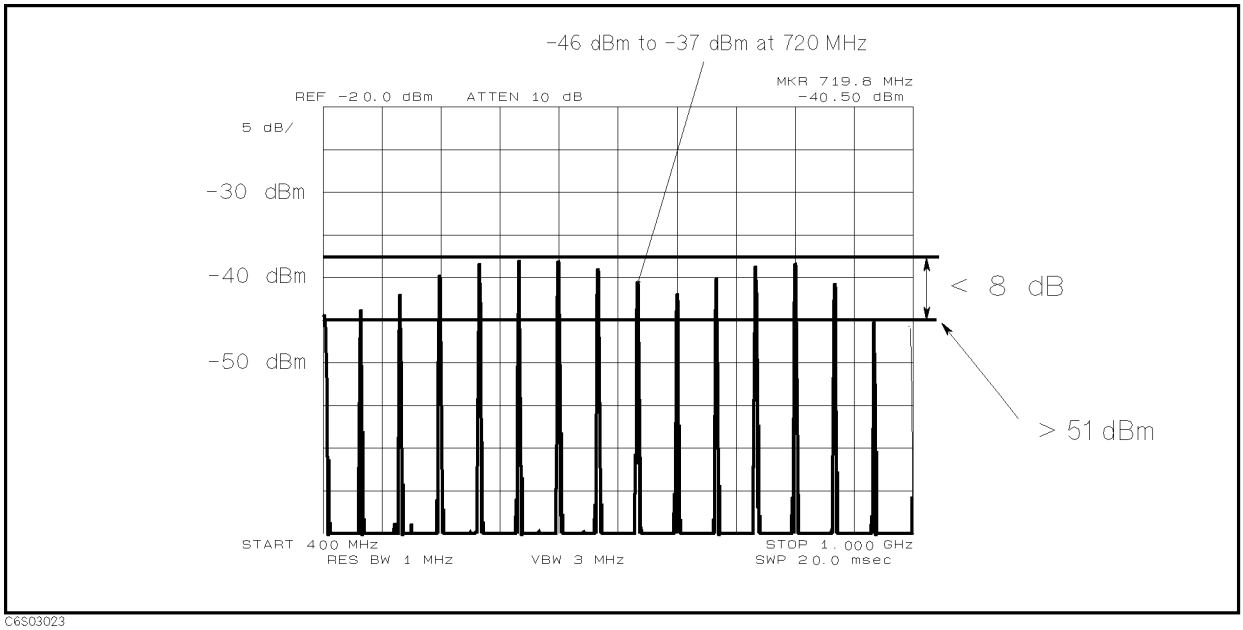
3. Set the spectrum analyzer as follows:

Start Frequency	400 MHz
Stop Frequency	1 GHz
RBW	1 MHz
Reference Level	– 20 dBm
Scale	5 dB/div

4. Turn the HP 4291B analyzer ON.
5. Adjust A5 “COMB DC BIAS ADJ” until the spectrum analyzer display indicates the following:

720 MHz Signal Level	between −46 and −37 dBm
480 MHz to 920 MHz Flatness	< 8 dBm
480 MHz to 920 MHz Signal Level	> −51 dBm

The adjustment location is shown in Figure 3-7. A typical spectrum analyzer display is shown in Figure 3-8.



C6S03023

Figure 3-8. Comb Generator Output

STEP PRETUNE CORRECTION CONSTANTS

The purpose of this procedure is to generate the correction constants that are used to pretune the step loop oscillator.

Required Equipment

None

Procedure

1. Run the adjustment program and display the main menu (see "UPDATING Correction Constants USING THE ADJUSTMENTS PROGRAM").
2. Choose the Step Pretune Correction Constants.
3. Follow the adjustment program instructions to update the correction constants.

SECOND LOCAL PLL LOCK ADJUSTMENT

The purpose of this procedure is to lock the second local Phase Lock Loop (PLL).

Required Equipment

Spectrum Analyzer	HP 8566A/B
BNC(f)-SMA(m) adapter	PN 1250-1548
N(m)-BNC(f) adapter	PN 1250-1476
BNC cable, 122 cm	PN 8120-1840

Procedure

1. Turn the HP 4291B analyzer OFF.
2. Remove the "D" cable from the A3A1 "ALC Out" connector. Remove the "I" cable from the A3A2 "Second Local Out" connector. The connector locations are shown in Figure 3-9.

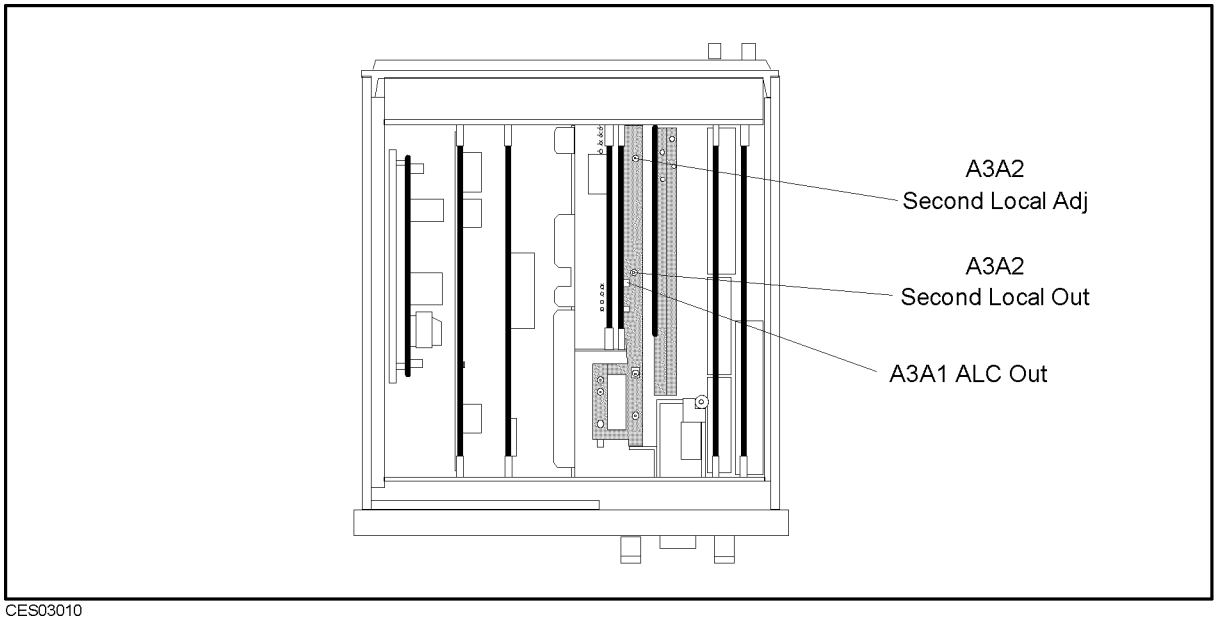


Figure 3-9. Second Local PLL Adjustment Location

3. Connect the equipment as shown in Figure 3-10.

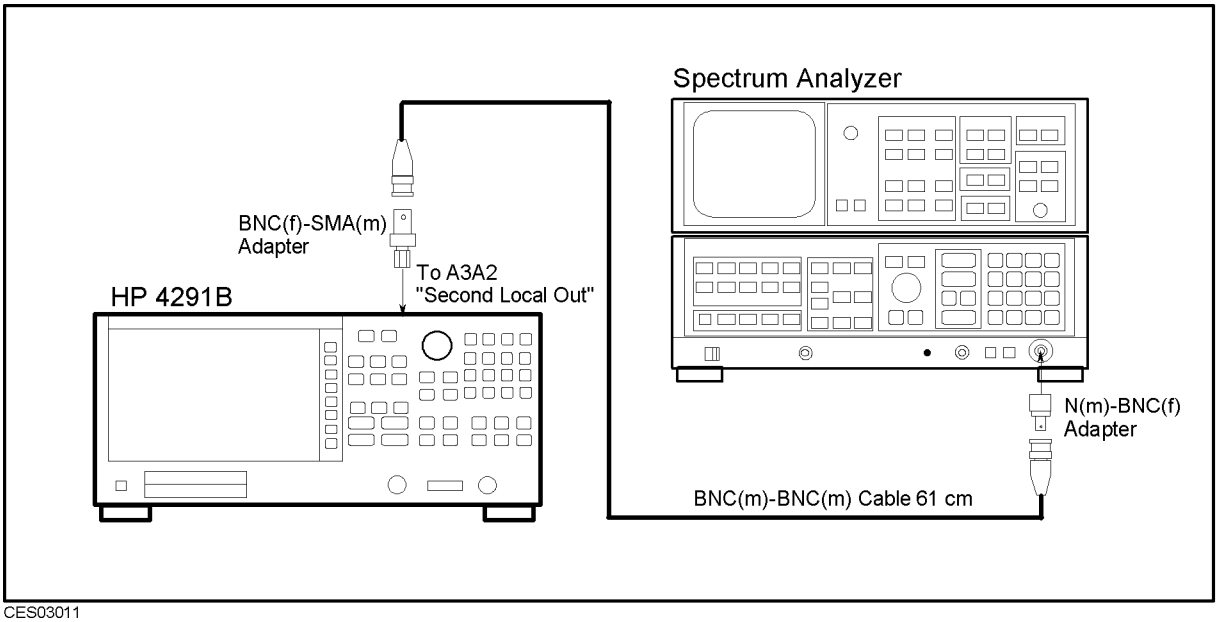


Figure 3-10. Second Local PLL Adjustment Setup

4. Set the spectrum analyzer as follows:

Center Frequency	2.08 GHz
Span	400 MHz
RBW	1 MHz

5. Turn the HP 4291B analyzer ON.
6. Press the following keys to execute adjustment Test No.37:

   (PRESET), (SYSTEM), SERVICE MENU, TESTS, (3), (7), (x1), EXECUTE TEST

7. Adjust A3A2 "Second Local Adj" until 2.08 GHz appears constantly on the spectrum analyzer display and the HP 4291B analyzer reading is between the limit lines. Then press CONT to complete the adjustment. If 2.24 GHz appears, rotate "Second Local Adj" clockwise. If 1.92 GHz appears, rotate "Second Local Adj" counterclockwise. The adjustment location is shown in Figure 3-9.
8. Turn the analyzer OFF.
9. Reconnect the "I" cable to the A3A2 "Second Local Out" connector. Reconnect the "D" cable to the A3A1 "ALC Out" connector.

SOURCE VCXO ADJUSTMENT

The purpose of this procedure is to optimize the source VCXO oscillation.

Required Equipment

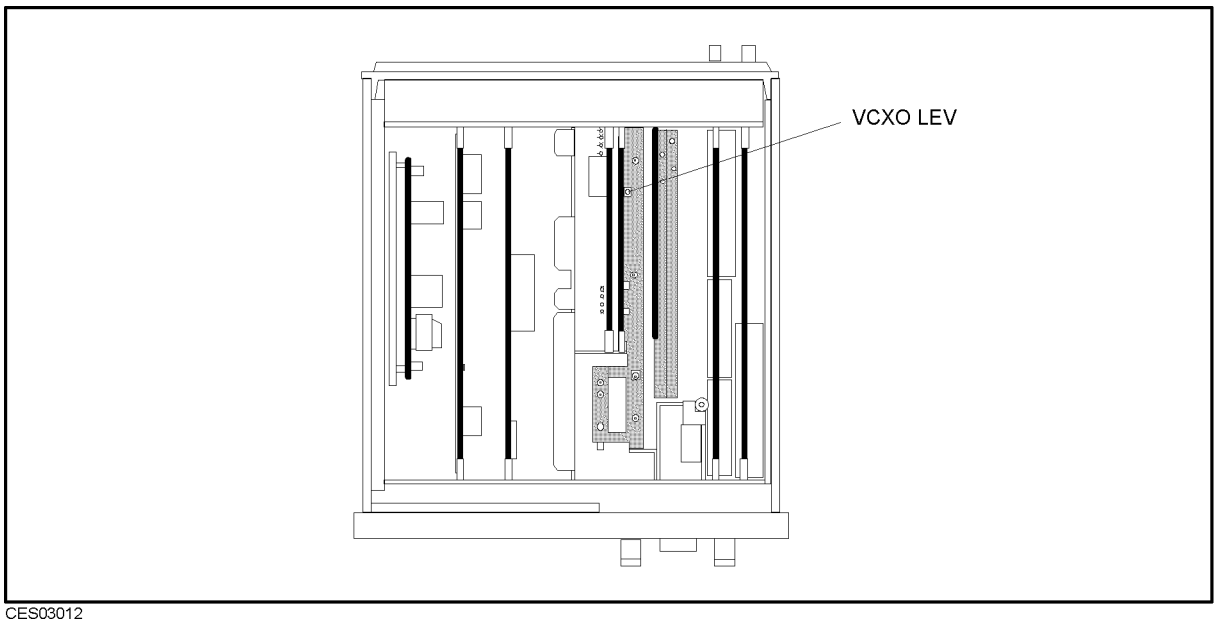
None

Procedure

1. Do not connect anything to the analyzer mainframe front terminals.
2. Press the following keys to execute adjustment Test No.39:

   (PRESET), (SYSTEM), SERVICE MENU, TESTS, (3), (9), (x1), EXECUTE TEST

3. Rotate "VCXO LEV" and confirm that a voltage peak appears during a rotation to confirm that the VCXO circuit is correct. Then press CONT.
4. Rotate "VCXO LEV" slowly to enable the instrument to memorize the peak voltage. Then press CONT.
5. Adjust "VCXO LEV" until the VCXO level is within the limits and "PASS" is displayed. Then press CONT to complete the adjustment.



CES03012

Figure 3-11. Source VCXO Adjustment Location

THIRD LOCAL VCXO ADJUSTMENT

The purpose of this procedure is to optimize the source VCXO oscillation.

Required Equipment

None

Procedure

1. Turn the analyzer OFF.
2. To gain access to the adjustment component, remove the side panel on the control keys side.
3. Do not connect anything to the analyzer mainframe front terminals.
4. Press the following keys to execute adjustment Test No.36:

   (PRESET), (SYSTEM), SERVICE MENU, TESTS, (3), (6), (x1), EXECUTE TEST

5. Rotate "VCXO ADJ" and confirm that two voltage peaks appear during a rotation to confirm that the VCXO circuit is correct. Then press CONT.
6. Rotate "VCXO ADJ" slowly to enable instrument to memorize the peak voltage. Then press CONT.
7. Adjust "VCXO ADJ" until the VCXO level is with in the limits and "PASS" is displayed. Then press CONT to complete the adjustment.

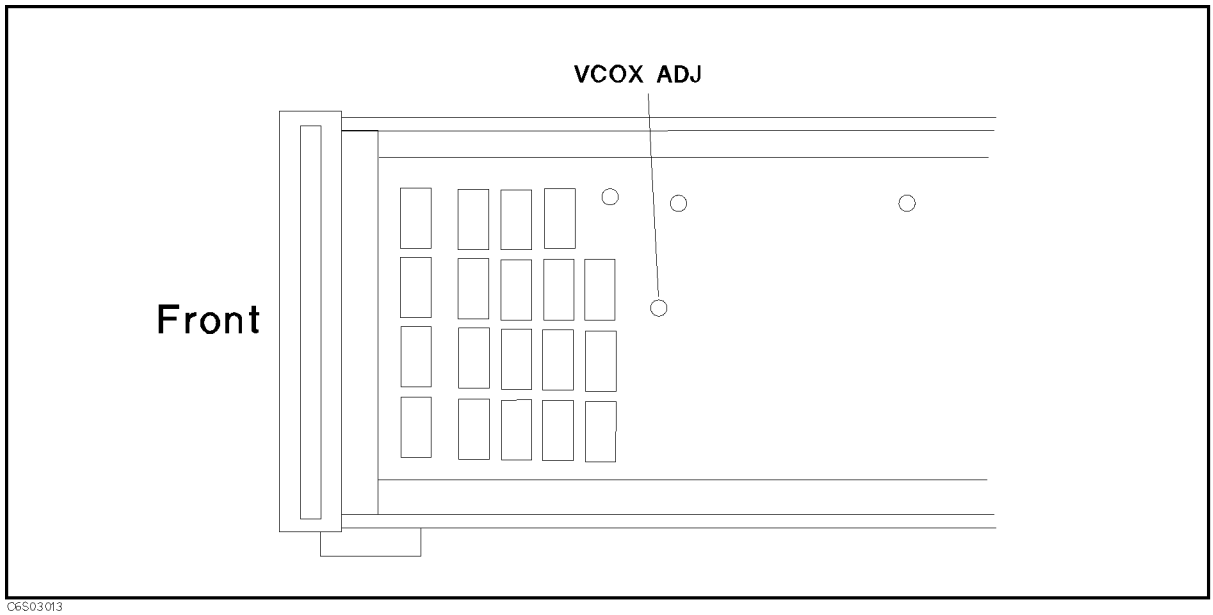


Figure 3-12. Third Local VCXO Adjustment Location

SOURCE MIXER LOCAL LEAKAGE ADJUSTMENT

The purpose of this procedure is to minimize the source mixer local leakage.

Required Equipment

Spectrum Analyzer ..... HP 8566A/B
N(m)-BNC(f) adapter (2 required) ..... PN 1250-1476
BNC cable, 122 cm (2 required) ..... PN 8120-1840

Procedure

1. Connect the equipment as shown in Figure 3-13.

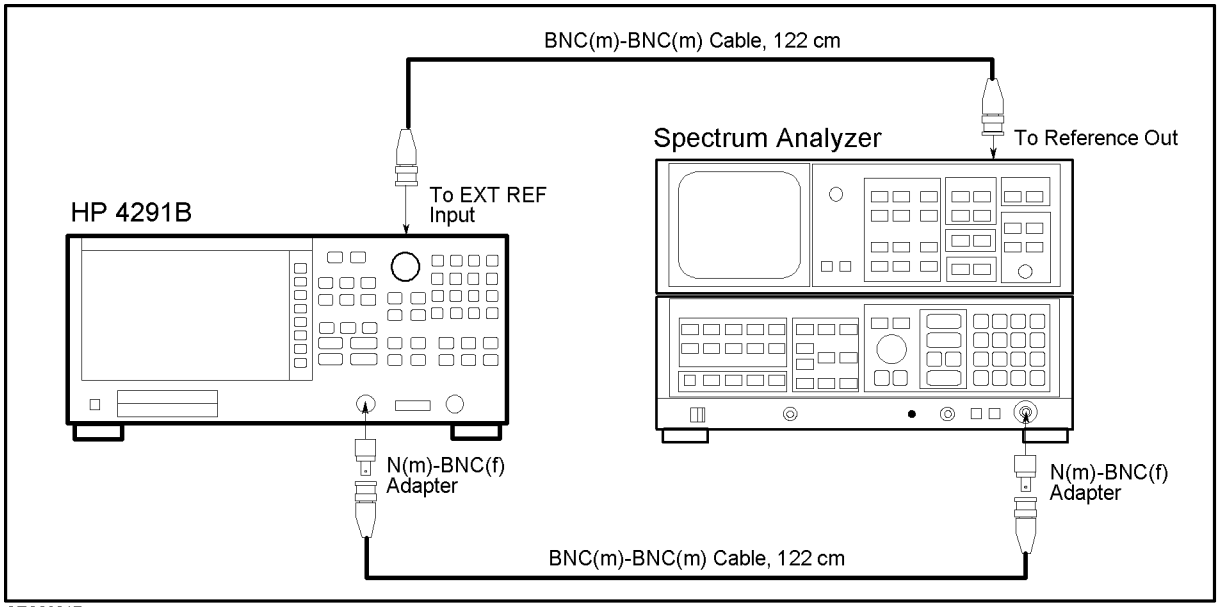


Figure 3-13. Source Mixer Local Leakage Adjustment Setup

2. Set the spectrum analyzer as follows:

Center Frequency	100 MHz
Span	100 MHz
RBW	300 kHz

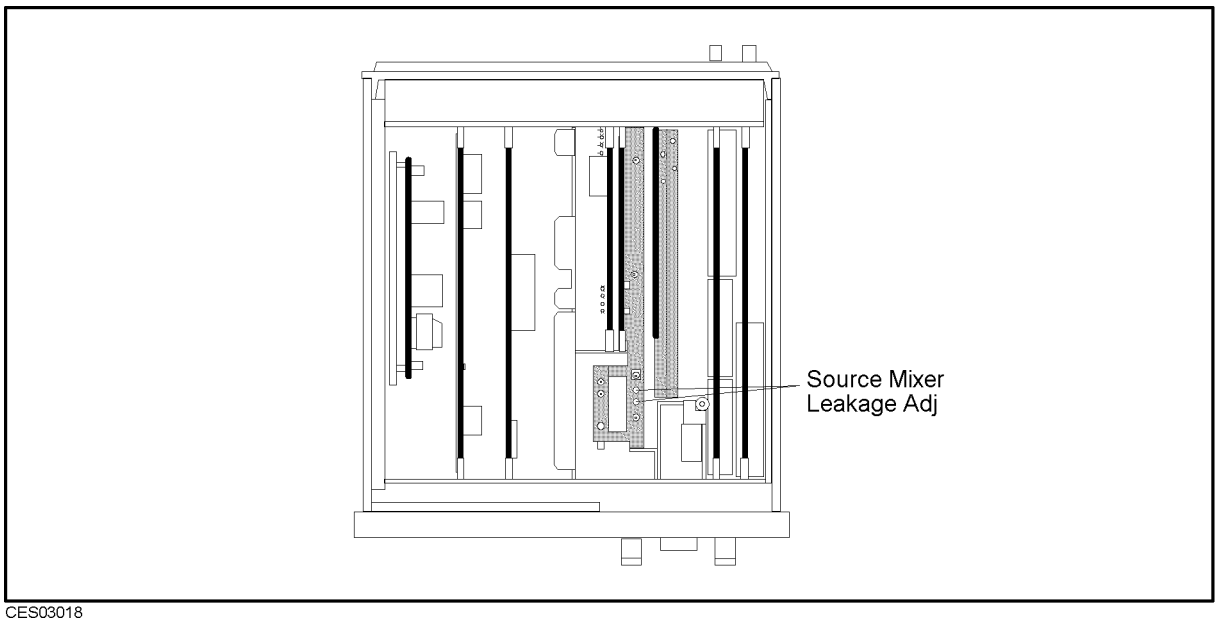
3. Press the following keys to execute adjustment Test No.38:

(PRESET), (SYSTEM), SERVICE MENU, TESTS, (3), (8), (x1), EXECUTE TEST

4. Adjust the local leakage adjustments until the spectrum analyzer reading of the 78.58 MHz signal level is smaller than −40 dBm. Then press CONT to complete the adjustment. The adjustment locations are shown in Figure 3-14.

Note

Carefully rotate the local leakage adjustments so that the adjustments are not misadjusted by much. It would be very difficult to recover from a large misadjustment.



CES03018

Figure 3-14. Source Mixer Leakage Adjustment Location

OSC LEVEL CORRECTION CONSTANTS

The purpose of this procedure is to obtain the correction constants that correct the OSC signal linearity and flatness.

Required Equipment

Power Meter ..... HP 436A
Power Sensor ..... HP 8482A

Procedure

1. Run the adjustment program and display the main menu (see "UPDATING Correction Constants USING THE ADJUSTMENTS PROGRAM").
2. Choose the OSC Level Correction Constants.
3. Follow the adjustment program instructions to update the correction constants. Figure 3-15 shows the equipment setup for the Correction Constants.

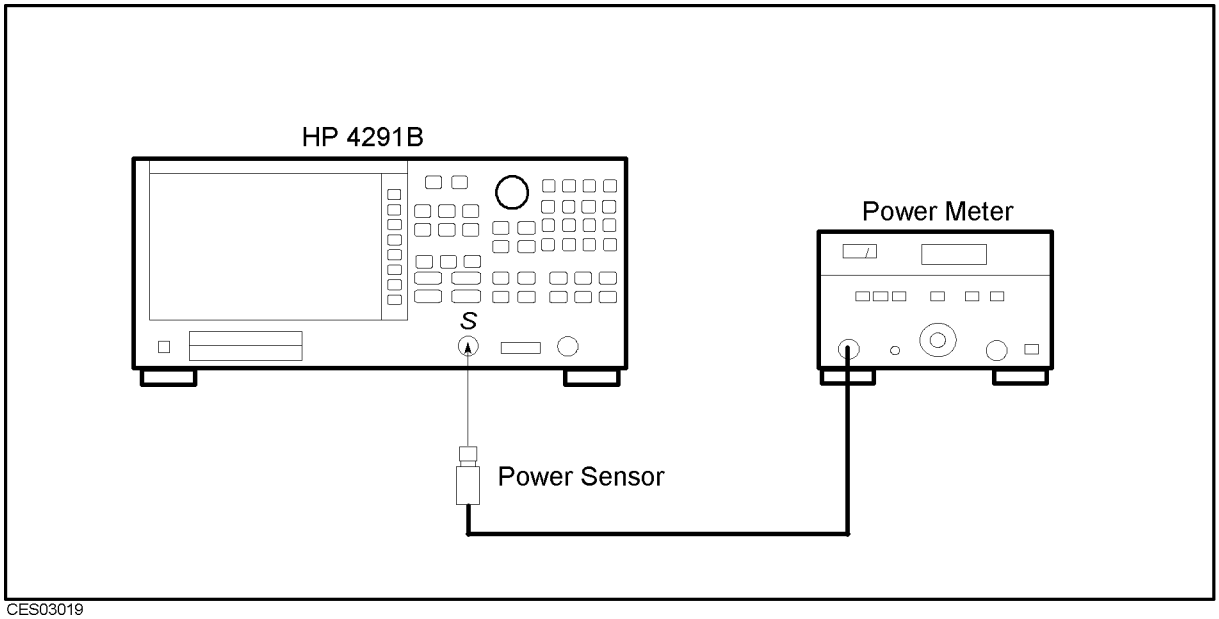


Figure 3-15. OSC Level Correction Constants Setup

HOLD STEP ADJUSTMENT

The purpose of this procedure is to minimize the hold step of the A6 receiver sample and hold output.

Required Equipment

None

Procedure

1. Turn the analyzer OFF.
2. To gain access to the adjustment component, remove the side panel on the control keys side.
3. Do not connect anything to the analyzer mainframe front terminals.
4. Turn the analyzer ON.
5. Press the following keys to execute adjustment Test No.34:

   (PRESET), (SYSTEM), SERVICE MENU, TESTS, (3), (4), (x1), EXECUTE TEST

6. Adjust "HOLD STEP ADJ" until the hold step level is within the limits and "PASS" is displayed. Then press CONT to complete the adjustment. The adjustment location is shown in Figure 3-16.

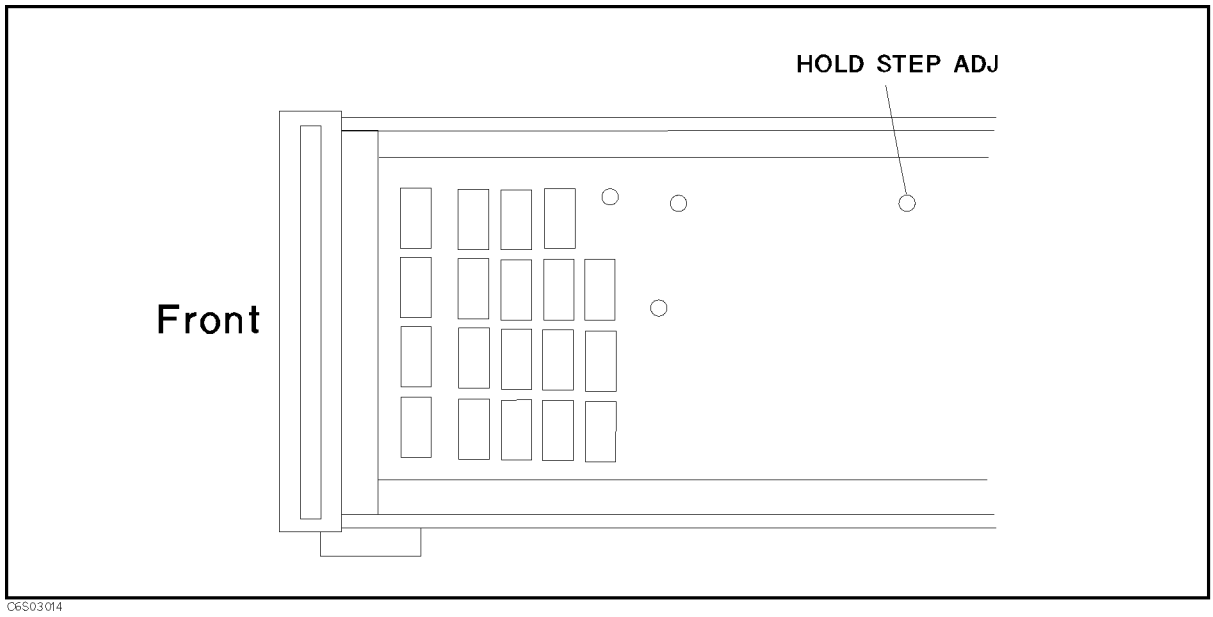


Figure 3-16. Hold Step Adjustment Location

BAND PASS FILTER ADJUSTMENT

The purpose of this procedure is to optimize the A6 receiver IF band pass filter.

Required Equipment

Type-N Cable, 61 cm .....HP 11500B or part of HP 11851B

Procedure

1. Turn the analyzer OFF.
2. To gain access to the adjustment component, remove the side panel on the control keys side.
3. Connect the equipment as shown in Figure 3-17.

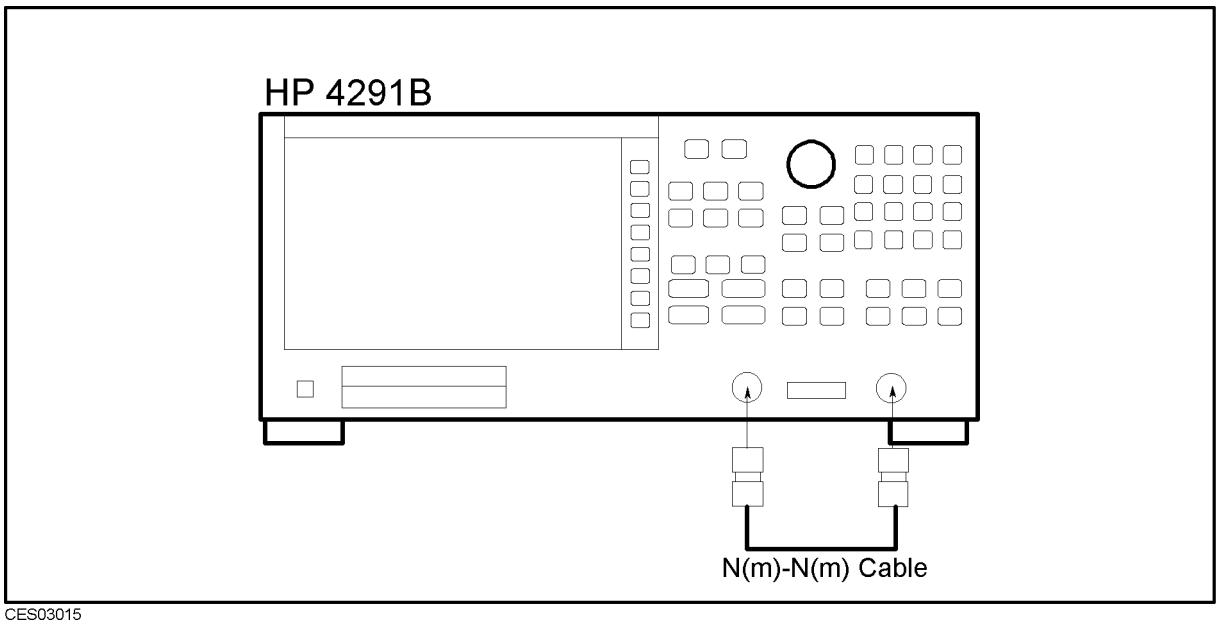


Figure 3-17. Band Pass Filter Adjustment Setup

4. Turn the analyzer ON.
5. Press the following keys to execute adjustment Test No.35:

   (PRESET), (SYSTEM), SERVICE MENU, TESTS, (3), (5), (x1), EXECUTE TEST

6. Adjust "BPF ADJ 1" to maximize the trace. Then adjust "BPF ADJ 2" to maximize the trace and press CONT to complete the adjustment. The adjustment location is shown in Figure 3-18. (The interaction of "BPF ADJ1" and "BPF ADJ 2" is negligible.)

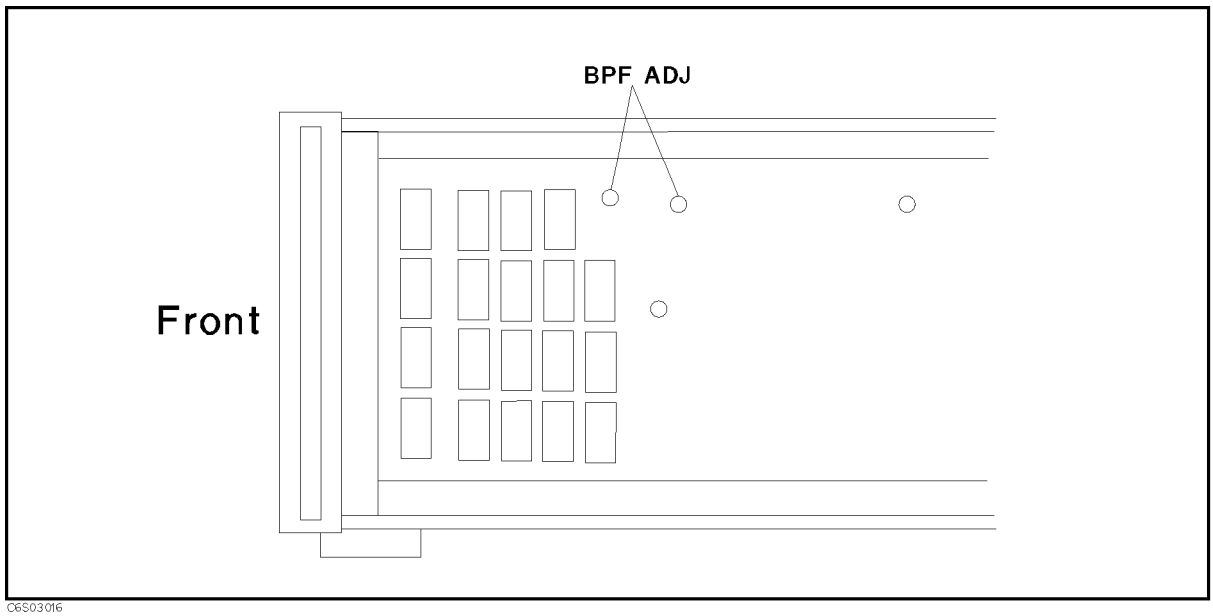


Figure 3-18. Band Pass Filter Adjustment Location

DC BIAS LEVEL CORRECTION CONSTANTS (OPTION 001 ONLY)

The purpose of this procedure is to obtain the correction constants that correct the DC bias voltage and current level.

Multimeter ..... HP 3458A
APC-7® -N(f) Adapter ..... HP 11524A
N(m)-BNC(f) Adapter ..... PN 1250-1476
BNC(f)-Banana Adapter ..... PN 1251-2277
BNC cable, 61 cm ..... PN 8120-1839

Procedure

1. Run the adjustment program and display the main menu (see "UPDATING Correction Constants USING THE ADJUSTMENTS PROGRAM").
2. Choose the DC Bias Correction Constants.
3. Follow the adjustment program instructions to update the correction constants. Figure 3-19 shows the equipment setup for the Correction Constants. the "GND" side of the BNC(f)-Banana adapter must be connected to the multimeter's "LO" terminal.

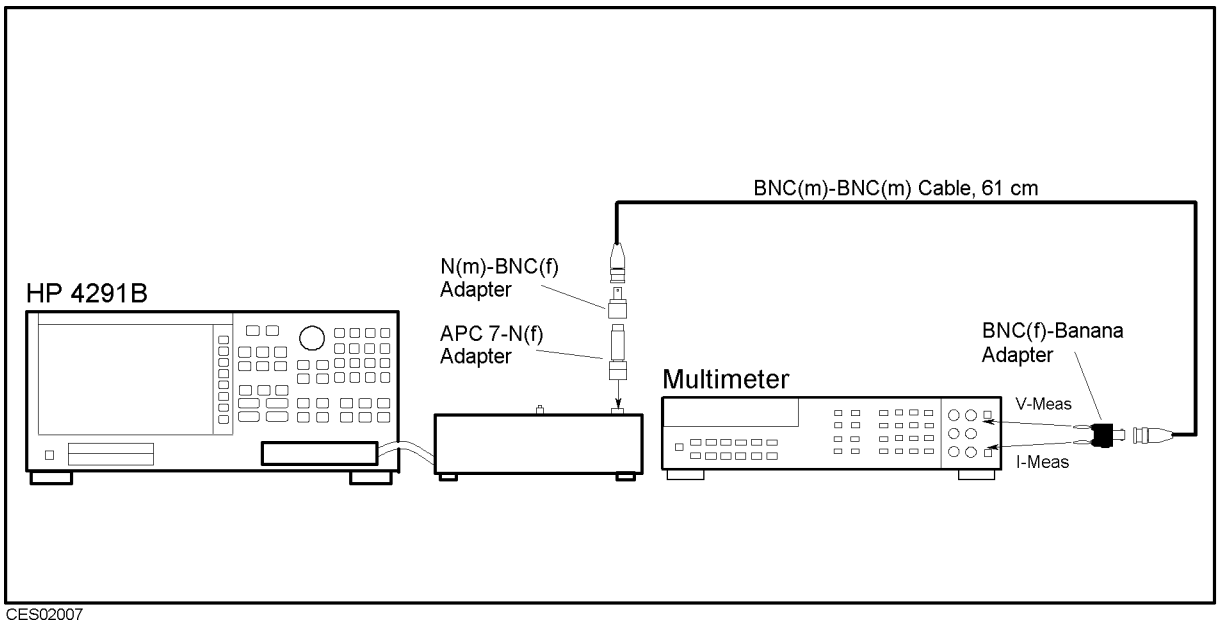


Figure 3-19. DC Bias Level Correction Constants Setup

10 MHz REFERENCE OSCILLATOR FREQUENCY ADJUSTMENT (OPTION 1D5 ONLY)

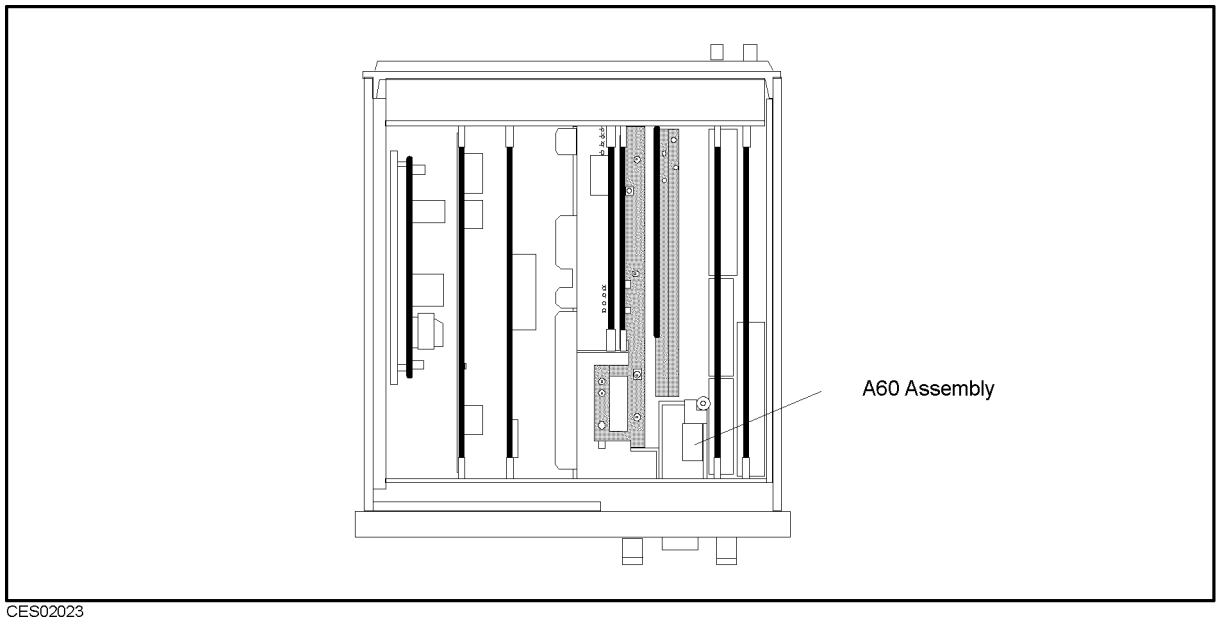
The purpose of this procedure is to adjust the 10 MHz high stability reference oscillator (Option 1D5) frequency.

Required Equipment

Frequency Counter	HP 5343A
Frequency Standard	HP 5061B
APC3.5(m)-APC3.5(f) adapter	PN 1250-1866
BNC(f)-SMA(f) adapter	PN 1250-0562
N(m)-BNC(f) adapter	PN 1250-1476
BNC cable, 61 cm (3 required)	PN 8120-1839

Procedure

1. Turn the analyzer OFF.
2. Pull the A60 assembly out. Place it on the analyzer with the bracket facing upward. The A60 location is shown in Figure 3-20.



CES02023

Figure 3-20. 10 MHz Reference Oscillator Frequency Adjustment Location

Note

The analyzer must be ON continuously for at least 24 hours immediately prior to the oscillator adjustment. This warm-up time allows both the temperature and frequency of the oscillator to stabilize. Failure to allow sufficient stabilization time could result in oscillator misadjustment.

3. Allow the analyzer to remain ON continuously for at least 24 hours to ensure that both the temperature and frequency of A60 can stabilize.

4. Connect a BNC(m)-BNC(m) cable between the "EXT REF" input connector and the "REF OVEN" connector on the analyzer rear panel. Then connect the equipment as shown in Figure 3-21.

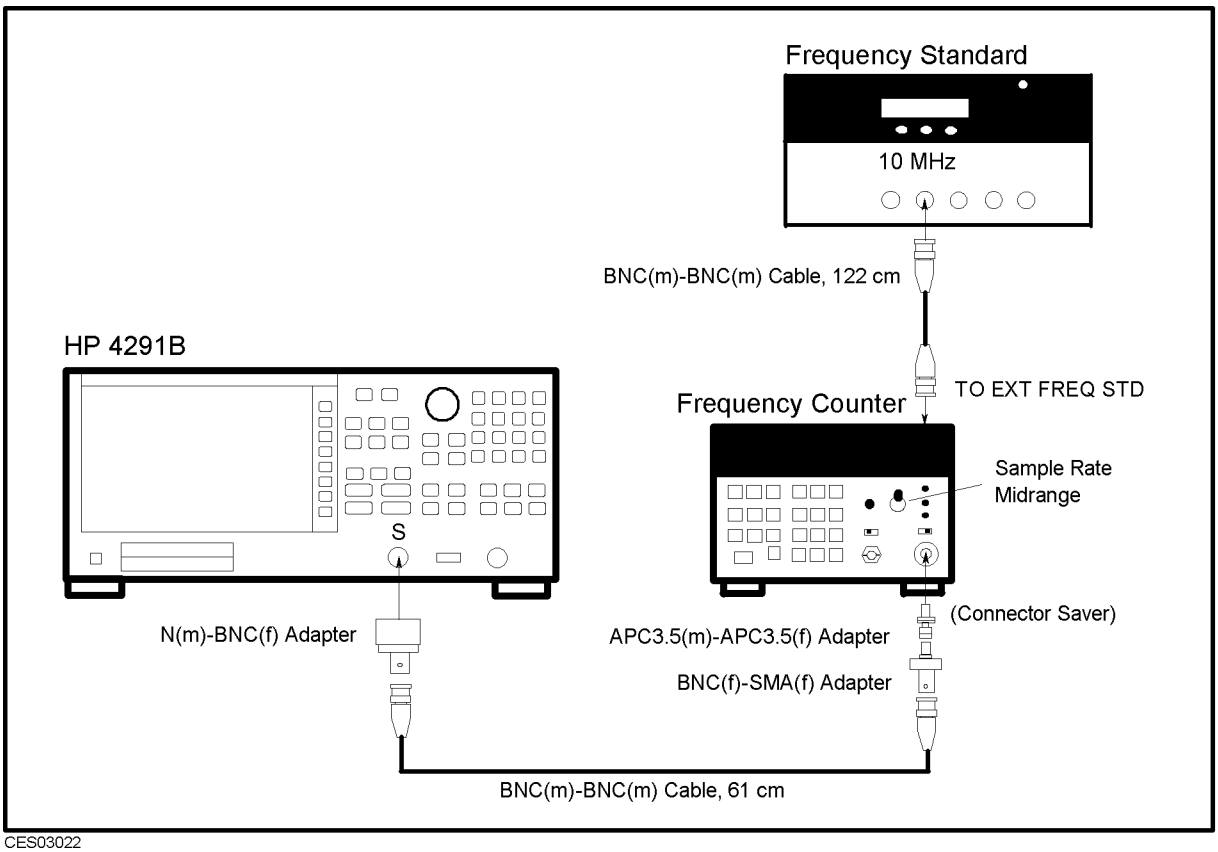


Figure 3-21. 10 MHz Reference Oscillator Frequency Adjustment Setup

5. Press (Preset) to initialize the analyzer. Then set the analyzer controls as follows:

Control Settings	Key Strokes
Frequency Span: 0 Hz	(Span), (0), (x1)
Center Frequency: 1.8 GHz	(Center), (1), (.), (8), (G/n)
Source Power: −33 dBm	(Source), POWER, (−), (3), (3), (x1)

6. Set the frequency counter as follows:

   Input Impedance 50 Ω
   Frequency Range 500 MHz - 26.5 GHz

7. Remove the dust cap screw on the A60 assembly to gain access to the adjustment screw.
8. Adjust the A60 adjustment screw until the frequency counter reading is within 1.8 GHz ± 1 Hz.
9. Turn the analyzer OFF.
10. Replace the dust cap screw into the A60 assembly, and replace the A60 assembly into the slot.

4

Overall Troubleshooting

This chapter consists of the following sections:

- Troubleshooting Summary
- Inspect the Power ON Sequence
- Verify Functional Groups
- Troubleshooting the HP-IB System

The *Troubleshooting Summary* outlines how to troubleshoot the HP 4291B using the troubleshooting flow diagram.

The *Inspect the Power ON Sequence* begins the troubleshooting procedures by inspecting the power on sequence.

The *Verify Functional Groups* provides verification procedures to isolate the problem to the faulty functional group.

Troubleshooting the HP-IB System gives some hints for troubleshooting when the HP 4291B is used in an HP-IB system.

TROUBLESHOOTING SUMMARY

The troubleshooting strategy of this manual is based on a verification (rather than symptomatic) approach. Verification procedures and the resulting corrective actions are given in the manual. By following these directions, you will determine the faulty assembly that must be replaced.

Figure 4-1 shows the overall troubleshooting flow. The following paragraphs provide brief descriptions of the troubleshooting sequence:

Troubleshooting is started by performing the inspecting the power on sequence.

Inspecting the power on sequence and verifying faulty groups indicate one or more faulty groups in the analyzer's five functional groups. (The analyzer can be divided into five functional groups: power supply, digital control, source, receiver, and transducer.)

A faulty assembly is isolated to a faulty functional group according to the troubleshooting procedure for each faulty group. The troubleshooting procedures are given in Chapters 5 to 9.

A faulty assembly is replaced according to Chapters 12 and 13. Chapter 12 lists the replaceable parts and Chapter 13 gives replacement procedures for the major parts.

The procedures required after assembly replacement, such as adjustments and performance tests, are given in Chapter 14.

Troubleshooting hints that can be used when the analyzer is used in an HP-IB system are given in this chapter. When the analyzer is used in an HP-IB system, the analyzer's HP-IB function needs to be verified as the first step in troubleshooting.

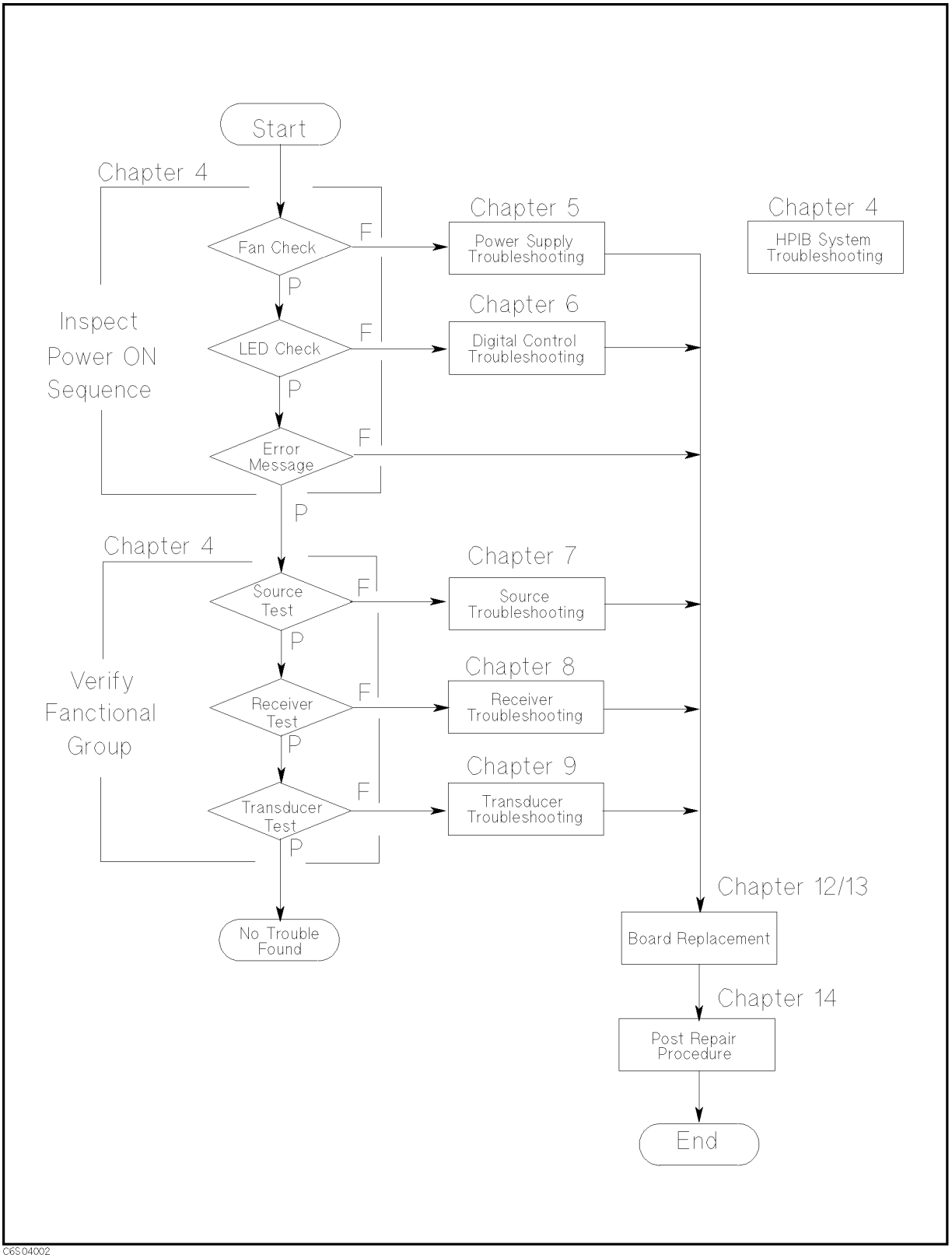


Figure 4-1. Overall Troubleshooting Flow

INSPECT THE POWER ON SEQUENCE

This section begins the troubleshooting procedures by inspecting the power on sequence.

Check the Fan

Turn the analyzer power on. Inspect the fan on the rear panel.

- The fan should be rotating and audible.

In case of unexpected results, check the AC line power to the analyzer. Check the fuse (the rating is listed on the rear panel). Check the line voltage setting. To set the line voltage, see the *Power Requirements* in Appendix B.

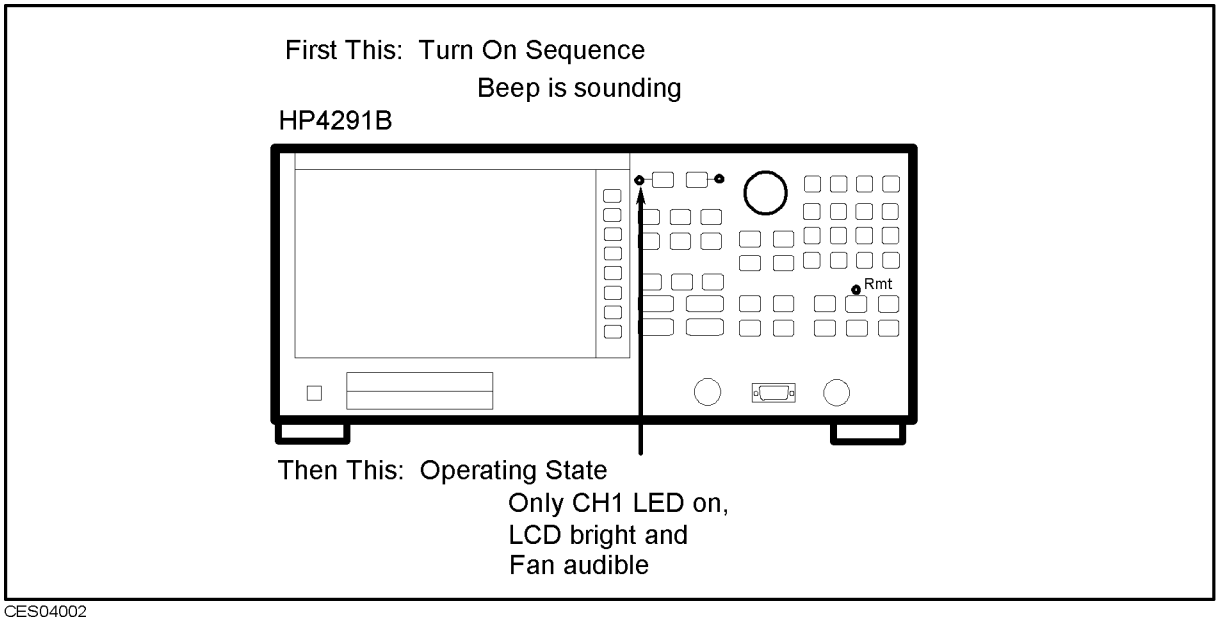
If the problem persists, continue with Chapter 5.

Check the Front Panel LEDs

Turn on the analyzer and watch for the following events in this order:

1. Beep sounds in about a second.
2. The Ch 1 LED turns on.
3. The display should come up bright and focused.

In case of unexpected results, continue with Chapter 6.



CES04002

Figure 4-2. Front Panel LEDs

Check Error Message

Turn the analyzer power on, and inspect the display. No error message should be displayed. If one of the error messages listed below is displayed, follow the related instructions. For any other message, see the *Error Messages* in the Messages appendix.

Error Messages	Instruction
POWER ON TEST FAILED	This indicates the power on self-test failed. Continue with *Troubleshooting When Power On Self-test Failed*
EEPROM CHECK SUM ERROR	This indicates that the correction constants stored in the EEPROM on the A1 CPU are invalid or the EEPROM is faulty. Continue with Chapter 6.
Svc (Status Annotation)	This indicates that the correction constants stored in the EEPROM on the A1 CPU are invalid or the EEPROM is faulty. Continue with Chapter 6.
POWER FAILED ON - - -	One or more of the A2 power supplies (+15 V, +8.5 V, +5.3 V, +5 V, -5 V, -15 V) is displayed in - - - of the message. The displayed power supplies are shutdown due to trouble on the A2 post-regulator. Continue with Chapter 5.
POWER FAILED ON PostRegHot	This indicates the A2 power supplies (+15 V, +8.5 V, +5.3 V, +5 V, -5 V, -15 V) are shutdown because the heat sink on the A2 post-regulator is too hot. Cool down the analyzer for about 30 minutes. Then turn the analyzer power on. If this message is still displayed, replace the A2 post-regulator.
PHASE LOCK LOOP UNLOCKED	This indicates one or more of the PLLs (phase lock loops) in the oscillators is not working properly. Continue with *Troubleshooting When Power On Self Test Failed* .

Troubleshooting When Power On Self-test Failed

Note

The analyzer performs the power on self-test every time the analyzer is turned on. In the power on self-test, internal diagnostic tests 1, 4, 5, 6, 7, and 9 through 16 are executed sequentially. The first failed test indicates the most probable faulty assembly. For more information about the internal tests, see Chapter 10.

If the power on self-test fails and the "POWER ON TEST FAILED" message is displayed, execute the ALL INT test, according to the following procedure, to identify the first failed test. Then replace the probable faulty assembly (see the Table 4-1).

a. Press (PRESET), (SYSTEM), SERVICE MENU, TESTS, (0), and (x1) to access internal test 0: ALL INT.
b. Press EXECUTE TEST to execute the ALL INT test.
c. Wait until the test result, PASS or FAIL, is displayed.
d. Press the (⇧), (⇩) keys to find the first occurrence of a FAIL message for tests 1 and 4 through 16.

Table 4-1. Troubleshooting Information for Internal Test Failure

Test No.	First Failed Test	Troubleshooting Information
1	A1 CPU	Replace A1 CPU.[1]
4	A2 POST REGULATOR	Continue with the *A2 POST REGULATOR Test Fail* section.
5	A6 A/D CONVERTER	The A6 receiver IF is the most probable faulty board. Replace the A6 receiver IF.
6	A5 REFERENCE OSC	The A5 synthesizer is the most probable faulty board. Replace the A5 synthesizer.
7	A5 FRACTIONAL N	The A5 synthesizer is the most probable faulty board. Replace the A5 synthesizer.
8	A5 STEP OSC	The A5 synthesizer is the most probable faulty board. Replace the A5 synthesizer.
9	A4A1 1ST LO OSC	The A4A1 1st LO OSC is the most probable faulty board. Replace the A4 1st LO/Receiver RF.
10	A3A2 2ND LO OSC	The A3A2 2nd LO OSC is the most probable faulty board. Replace the A3A2 2nd LO.
11	A3A1 DIVIDER	The A3A1 Source Vernier is the most probable faulty board. Replace the A3A1 Source Vernier.
12	A6 3RD LO OSC	The A6 receiver IF is the most probable faulty board. Replace the A6 receiver IF.
13	A3A1 SOURCE OSC	The A3A1 Source Vernier is the most probable faulty board. Replace the A3A1 Source Vernier.
14	A6 SEQUENCER	The A6 receiver IF is the most probable board. Replace the A6 receiver IF.
15	SOURCE LEVEL	Continue with Chapter 7.
16	DC BIAS	A22 DC Bias 1/2 or A23 DC Bias 2/2 is probably faulty, continue with *CHECK A22 DC BIAS 1/2 OUTPUT* in Chapter 7.

1 EEPROM with data needs to be placed, see Chapter 13.

A2 POST REGULATOR Test Fail

If internal test 4: A2 POST REGULATOR is the first failed test, the power supply functional group is the most probable faulty group. See Chapter 5.

Also, the test failure might be caused by A6 A/D converter trouble. Execute internal test 5: A6 A/D CONVERTER to verify the A/D converter by performing the following procedure. If the test 5 fails, suspect the A5 synthesizer and A6 receiver IF in addition to the power supply functional group.

i. Press (5), (x1), EXECUTE TEST to execute internal test 5: A6 A/D CONVERTER.
ii. Wait until the test result, PASS or FAIL, is displayed.

VERIFY FUNCTIONAL GROUPS

This section provides faulty group isolation procedures.

Source Test

Verify the source group operation by performing following procedure.

Test Equipment

Frequency Counter	HP 5343A Option 001
Power meter	HP 436A Opt. 022, HP 437B, or HP 438A
Power Sensor	HP 8482A
BNC cable, 61 cm	PN 8120-1839
N(m)-BNC(f) adapter	PN 1250-1476

Procedure

1. Perform the frequency accuracy test according to Chapter 2.
   - If the test fails, go to Chapter 7.
2. Calibrate the power meter for the power sensor.
3. Connect the equipment as shown in Figure 4-3.

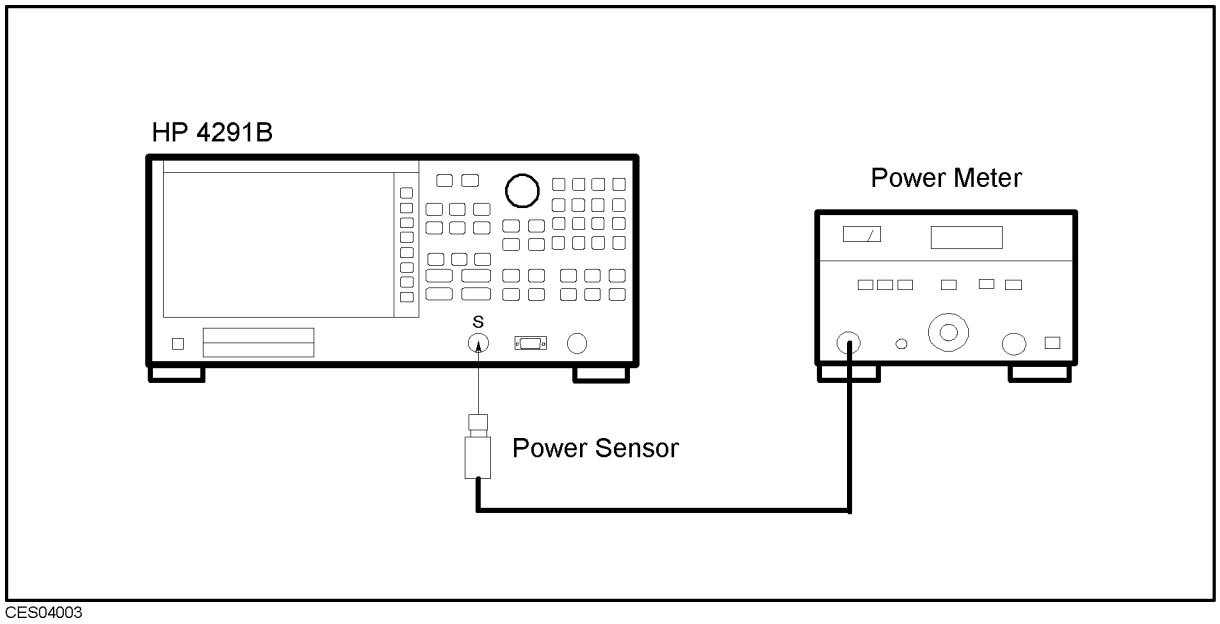


Figure 4-3. Source Test Setup

4. Turn the analyzer power on.
5. Press (SYSTEM), SERVICE MENU, SERVICE MODES, CORRECTION CONSTANTS, OSC LVL CC, FRONT to select the source correction constants for the front output connector.
6. Press (Source), OSC UNIT, dBm, (—), (1), (9), (x1) to set the OSC level to −19 dBm.
7. Press (Span), (0), (x1), (Center), (1), (M/μ) to set the frequency to 1 MHz.

8. Confirm that the power meter reading is within the test limits shown in Table 4-2.

Table 4-2. Source Test Settings

Frequency	Osc Level	Test Limit
1 MHz	–19 dBm	± 2 dB
10 MHz	–13 dBm	± 2 dB
100 MHz	–7 dBm	± 2 dB
1 GHz	7 dBm	± 2 dB
1.8 GHz	1 dBm	± 3 dB

9. Perform the test for all settings listed in Table 4-2.
   - If the test fails, perform the OSC level correction constants according to Chapter 3. If the test still fails, go to Chapter 7.
   - If the test passes, continue with the next step.
10. Press (Center), (1.8) to set the frequency to 1.8 GHz.
11. Press (SYSTEM), `Service Menu`, `Service Modes`, `OSC`, `OSC AUTO man` and verify the label changes to `OSC auto MAN` to set the analyzer manual OSC level mode.
12. Press `OUTPUT ATT [AUTO]`, `10 dB` ,(then the label changes to `OUTPUT ATT [10 dB]`) to set the output attenuator to 10 dB.
13. Press `OSC DAC AUTO man` and verify the label changes to `OSC DAC auto MAN`. Then press `OSC DAC VALUE`, (3), (2), (0), (0), (0), (x1) to set the DAC value to 32,000.
14. Confirm that the power meter reading is greater than 2.5 dBm.
    - If the test fails, go to Chapter 7.
    - If the test passes, continue with the *Receiver Test* procedure.

Receiver Test

Verify the receiver operation by performing following procedure.

Test Equipment

Type-N Cable, 61 cm .....HP 11500B or part of HP 11851B

Procedure

1. Verify that nothing is connected to the front panel of the analyzer mainframe.
2. Turn the analyzer power on.
3. Press (PRESET) to initialize the analyzer.
4. Press (SYSTEM), SERVICE MENU, TESTS, (2), (2), (x1) to access the RECEIVER GAIN test. When "RECEIVER GAIN" is displayed, press EXECUTE TEST.
5. Perform the test according to the displayed instructions.
   - If the test fails, go to Chapter 8.
6. Press (↑) to access the A6V/I NORMALIZER test. When "A6V/I NORMALIZER" is displayed, press EXECUTE TEST.
7. Perform the test according to the displayed instructions.
   - If the test fails, replace A6 receiver IF.
8. Press (↑) to access the FRONT ISOL'N test. When "FRONT ISOL'N" is displayed, press EXECUTE TEST.
9. Perform the test according to the displayed instructions.
   - If the test fails, go to Chapter 8. If the test passes, continue with the *Transducer Test* procedure.

Transducer Test

Verify the transducer operation by performing following procedures.

Test Equipment

Calibration Kit ..... HP 4291B furnished accessory

Procedure

Note

The HP 4291B has the following four test heads (including the optional test heads). Perform this test for all the available test heads.

- High impedance test head (Standard)
- Low impedance test head (Option 012)
- High temperature high impedance test head (Option 013)
- High temperature low impedance test head (Option 014)

1. Connect the test station to the mainframe. Then connect the test head to the test station as shown in Figure 4-4.

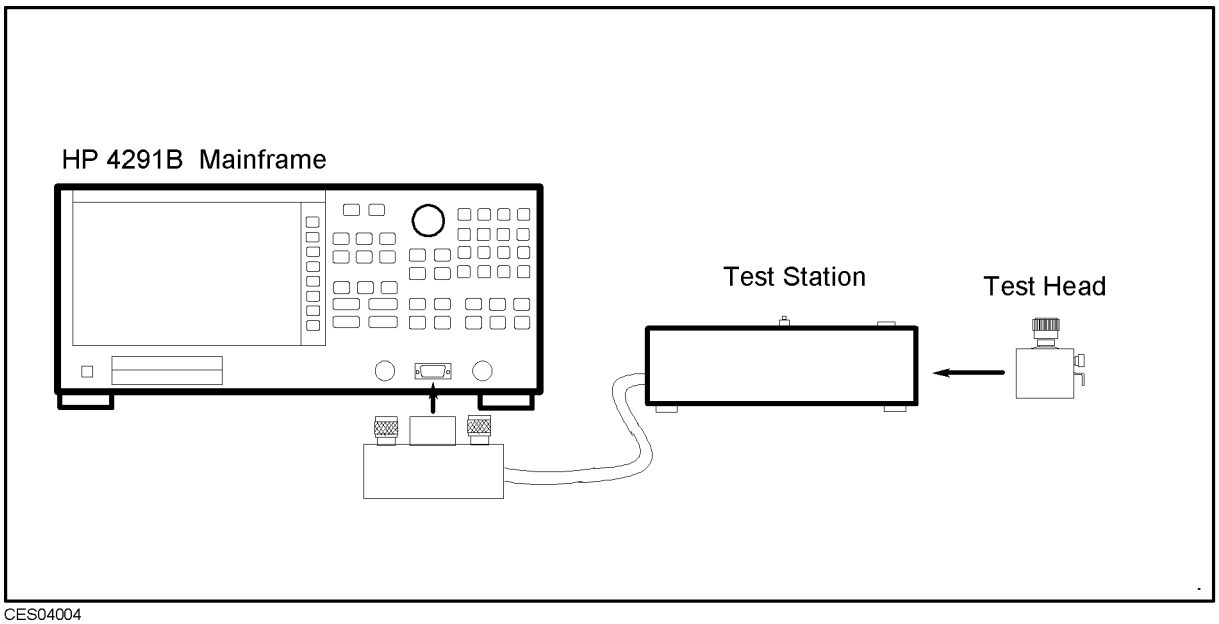


Figure 4-4. Transducer Test Setup

2. Turn the analyzer power on.
3. Press (SYSTEM), SERVICE MENU, TESTS to enter test display.
4. Select the test according to the test head to be verified, using the numeric keys and the (x1) key. Table 4-3 lists the test head tests and the test numbers.

Table 4-3. Test Head Tests List

Test Number	Test Name
30	HI Z HEAD
31	LO Z HEAD
32	HI TEMP HI Z HEAD
33	HI TEMP LO Z TEST

5. Press `EXECUTE TEST` and perform the test according to the displayed instructions.

   - If the test fails, go to Chapter 9. If the test passes, perform the test for the other available test heads in the same manner. If all the tests pass, the analyzer is probably operating correctly

INSPECT THE REAR PANEL FUNCTION

If the analyzer is operating unexpectedly after these checks are verified, continue with *Digital Control Troubleshooting* chapter.

Check the HP-IB Interface

If the unexpected operations appear when controlling the analyzer with an external controller, perform the following checks to verify the problem is not with the controller.

- Compatibility, must be HP 9000 series 200/300, see the manuals of the controller and the BASIC system.
- HP-IB interface hardware must be installed in the controller, see the manuals of the controller and the BASIC system.
- I/O and HP-IB binaries loaded, see the manuals of the BASIC system.
- Select code, see the manuals of the BASIC system.
- HP-IB cables, see the manuals of the BASIC system.
- Programming syntax, see the manuals of the BASIC system.

Check the Parallel Interface

Check the analyzer's Parallel Interface with a known working printer.

1. Connect a known working printer to the PRINTER port on the HP 4291B's rear panel.
2. Press (Copy) `PRINT [STANDARD]` to print.

Check the mini DIN Keyboard Connector

Check the analyzer's mini DIN Keyboard Connector with a known working keyboard.

1. Connect a known working mini DIN keyboard to the KEYBOARD connector on the HP 4291B's rear panel.
2. Press (Display), `DISPLAY ALLOCATION`, `HALF INSTR HALF BASIC`, then type any keys of the keyboard.
   - If the typed characters are displayed on the LCD, the Keyboard connector is working in the analyzer.
   - If the result is not correct, continue with *Digital Control Troubleshooting* chapter.

5

Power Supply Troubleshooting

INTRODUCTION

Use this procedure only if you have read *Troubleshooting*, and you believe the problem is in the power supply. The procedure is designed to let you identify the bad assembly within the power supply functional group in the shortest possible time.

The power supply functional group consists of:

- A40 Pre-Regulator
- A50 DC-DC Converter
- A2 Post-Regulator

All assemblies, however, are related to the power supply functional group because power is supplied to each assembly. Figure 5-1 shows all power lines in simplified block diagram form. For more information about the signal paths and specific connector pin numbers, see Figure 5-12, Figure 5-13, and Figure 5-14 at the end of this chapter.

If an assembly is replaced, see Chapter 14. It tells what additional tests or adjustments need to be done after replacing any assembly.

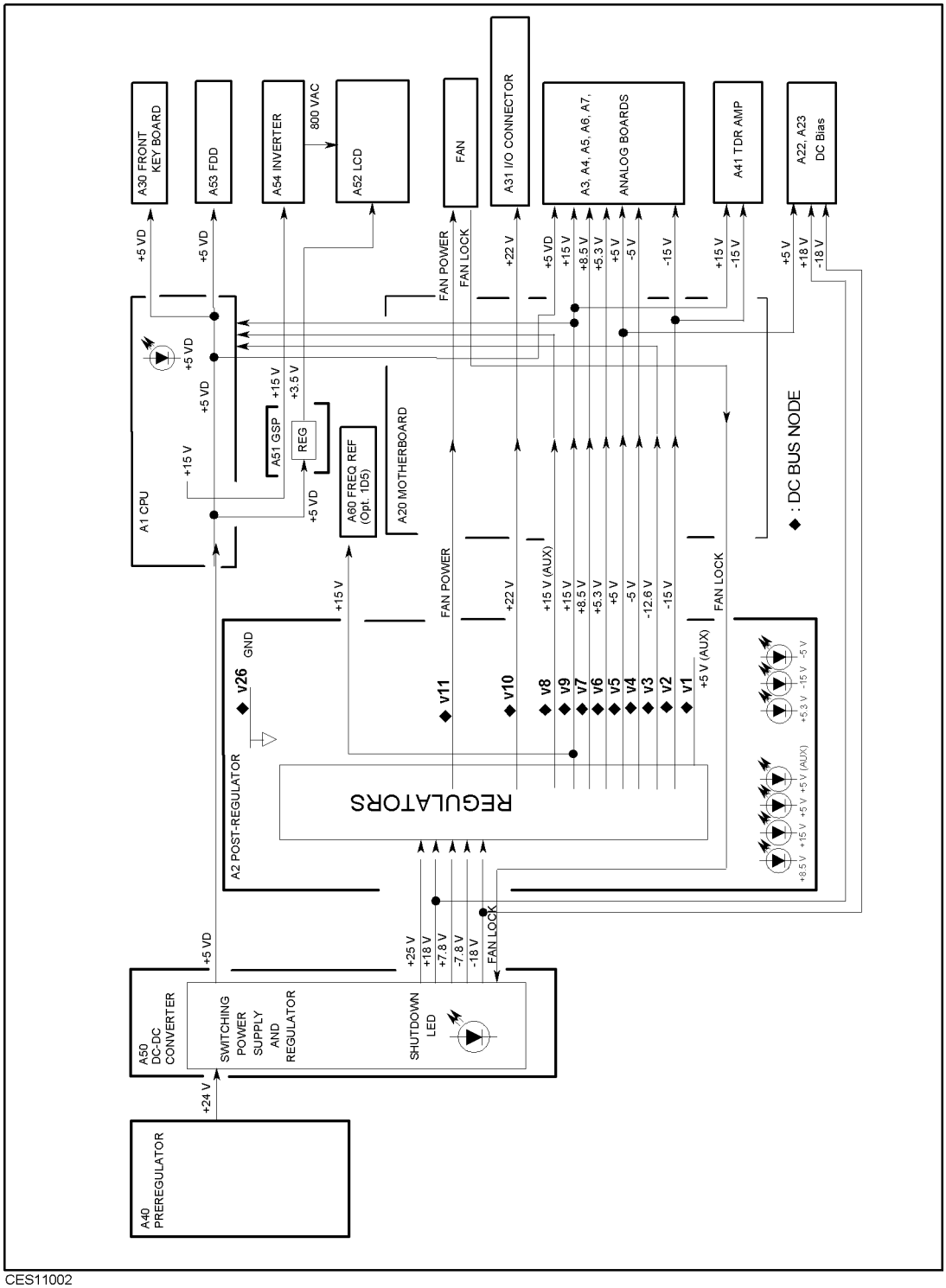


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Figure 5-1. Power Supply Lines Simplified Block Diagram

START HERE

1. Check Error Messages

Turn the analyzer power on. If one of error messages listed below appears on the display, follow the instruction of the displayed error message. If no error message is displayed, continue with *Check the Fan is Rotating.*

Error Messages	Instruction
`POWER FAILED ON - - -`	One or more of the A2 power supplies (+15 V, +8.5V, +5.3 V, +5 V, -5 V, -15 V) are displayed in - - - of the message. The displayed power supplies are shut down because of trouble on the A2 post-regulator. Continue with *CHECK THE A2 EIGHT LEDs* in this *START HERE.*
`POWER FAILED ON PostRegHot`	This indicates the A2 power supplies (+15 V, +8.5 V, +5.3 V, +5 V, -5 V, -15 V) are shut down because the hot heat sink on the A2 post-regulator is too hot. Cool down the analyzer for about 30 minutes. Then turn the analyzer power on. If this message is still displayed, replace A2 post-regulator.

These messages are associated with the power supply functional group. These messages indicate the A2 protective shutdown circuit is shutting down some of the A2 power supplies to protect them from over current, over voltage, under voltage, or too hot conditions. For more information about the A2 shutdown circuit, see Figure 5-13 Power Supply Block Diagram 2.

Note

These messages are displayed only after the power on sequence. When one of these messages is displayed, the analyzer's front-panel keys are disabled. In the power on sequence, the analyzer checks the shutdown status of the A2 power supplies (+15 V, +5 V, -5 V, -15 V). If a power supply is shutdown, the analyzer displays an error message and stops its operation. Once the analyzer stops the operation, all front-panel key operations are disabled. The only way to reset the analyzer is by turning the analyzer power off.

2. Check the Fan is Rotating

Look at the fan on the rear panel. Check the fan is rotating.

- If the fan is not rotating, continue with *FIND OUT WHY THE FAN IS NOT ROTATING* in this chapter.
- If the fan is rotating, continue with *Check the A50 SHUTDOWN LED.*

3. Check the A50 SHUTDOWN LED

There is a SHUTDOWN LED on the A50 DC-DC Converter. Perform the following procedure to check it. The SHUTDOWN LED is described in the *A50 SHUTDOWN LED* paragraph.

a. Turn the analyzer power off.

b. Remove the analyzer's top cover and shield plate.

c. Turn the analyzer power on.

d. Look at the A50 SHUTDOWN LED. The LED is normally on. Figure 5-2 shows the SHUTDOWN LED location on the A50 DC-DC Converter.

- If the A50 SHUTDOWN LED is off, check the cable connection between A40J2 and A2J4. If the connection is good, continue with *FIND OUT WHY THE A50 SHUTDOWN LED IS ON* in this chapter.
- If the A50 SHUTDOWN LED is on, continue with *Check the A1 +5 VD LED* in this procedure.

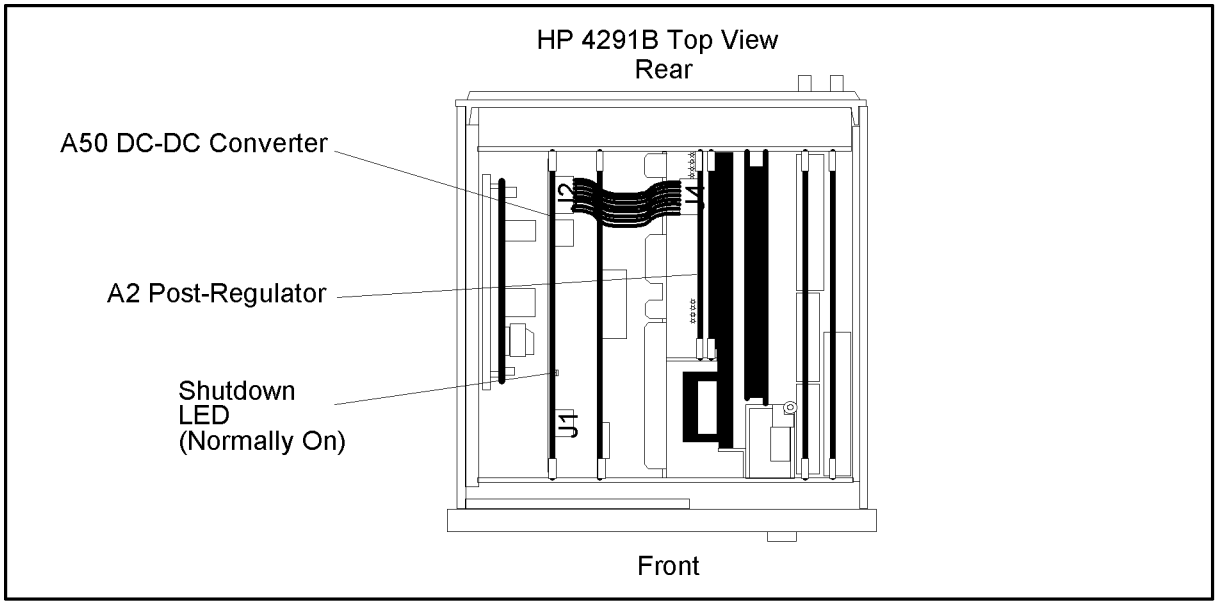

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Figure 5-2. A50 SHUTDOWN LED Location

A50 SHUTDOWN LED

The A50 SHUTDOWN LED turning off indicates some of A50 power supply is shut down by the A50 shutdown circuitry.

There are two FAN conditions, rotating and not rotating when the SHUTDOWN LED turns off. When the fan is rotating, the shutdown circuit is probably activated by the over current condition on the power lines in the A50 DC-DC Converter or the A2 Post Regulator. In this condition, though the A50 power supplies, +24 V, +5 VD, +18 V, +7.8 V, -7.8 V, and -18 V are shut down, the Fan Power +24 V is still supplied to the fan. When the fan is not rotating, the shutdown circuit is probably activated by the FAN LOCK signal missing.

For more information about the A50 SHUTDOWN circuit operation, see Figure 5-12 Power Supply Block Diagram 1.

Note Once the A50 SHUTDOWN circuit is activated, the only way to reset the circuit is turning the analyzer power off. Wait a minute after turning the analyzer off. Then turn it on.

4. Check the A1 +5 VD LED

a. Remove the analyzer's bottom cover.

b. Turn the analyzer power on.

c. Look at the +5 VD LED. Figure 5-3 shows the +5 VD LED location on A1 CPU. The LED is normally on.

- If the +5 VD LED is off, continue with *TROUBLESHOOT +5 VD POWER SUPPLY* in this chapter.
- If the +5 VD LED is on, the +5 VD power supply is verified with a 95% confidence level. Continue with *Check Eight A2 LEDs* in this procedure. If you want to confirm the last 5% uncertainty, perform the *Measure the A1 +5 VD Voltage* procedure.

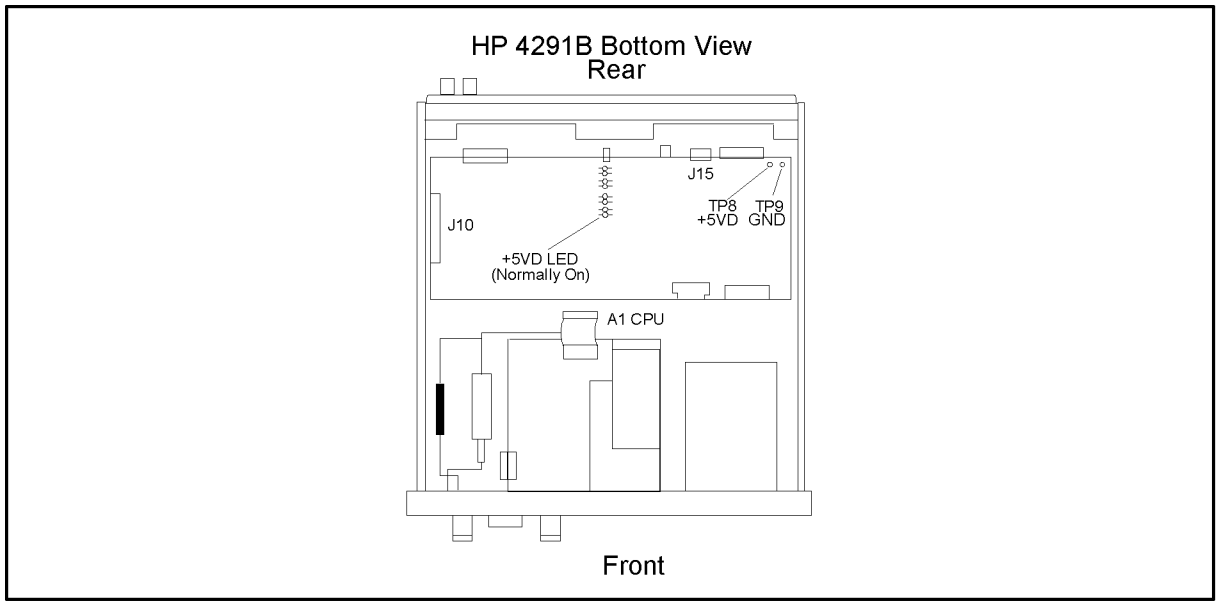

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Figure 5-3. A1 +5 VD LED Location

Measure the A1 +5 VD Voltage

Measure the DC voltage at test point A1TP8 (+5 VD) using a voltmeter. Check the voltmeter reading is within 4.59 V to 5.61 V.

- If the voltmeter reading is out of limits, continue with *FIND OUT WHY THE A1 LED IS NOT ON STEADILY*.
- If the voltmeter reading is within limits, continue with the next step.

5. Check the Eight A2 LEDs

a. Remove the analyzer's top cover and shield.

b. Turn the analyzer power on.

c. Look at all eight A2 LEDs. The A2 LED locations are shown in Figure 5-4. Check the LEDs are correctly on.

- If two or more LEDs are off, continue with *TROUBLESHOOT A2 POST-REGULATOR* in this chapter.

- If the LEDs are correctly on, continue with *Run the Internal Test 4: A2 POST REGULATOR*.

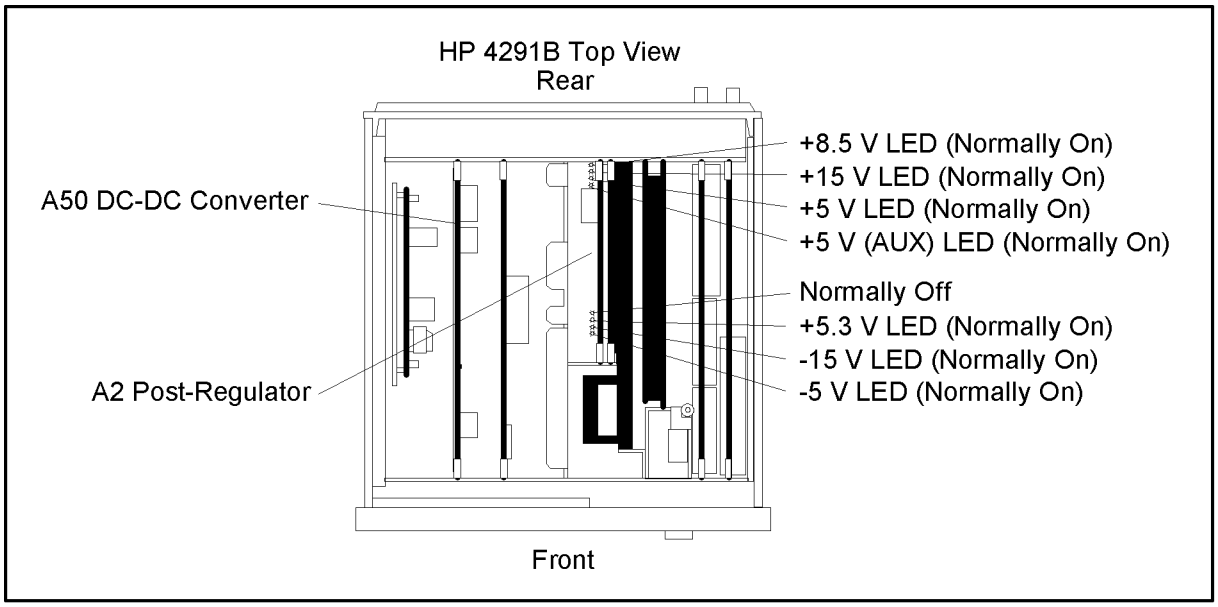

Figure 5-4. Eight A2 LED Locations

6. Run Internal Test 4: A2 POST REGULATOR

Internal test 4: A2 POST REGULATOR verifies the A2 post-regulator. Perform the following procedure to check the A2 post-regulator. Internal test 4 is described in *Internal Test 4: A2 POST REGULATOR*.

Note

Internal test 4: A2 POST REGULATOR is a built-in diagnostic test. The test checks all A2 power supply voltages within limits using the DC BUS and the A/D converter on the A6 receiver IF. If a power supply failure is found, the analyzer stops the test process and displays the test result as shown in Figure 5-5. For more information about the internal test and the DC BUS, see Chapter 10.

Press (System), SERVICE MENU, TESTS, (4), (x1), EXECUTE TEST to execute internal test 4: A2 POST REGULATOR. After the test is completed, the test result is displayed as shown in Figure 5-5.

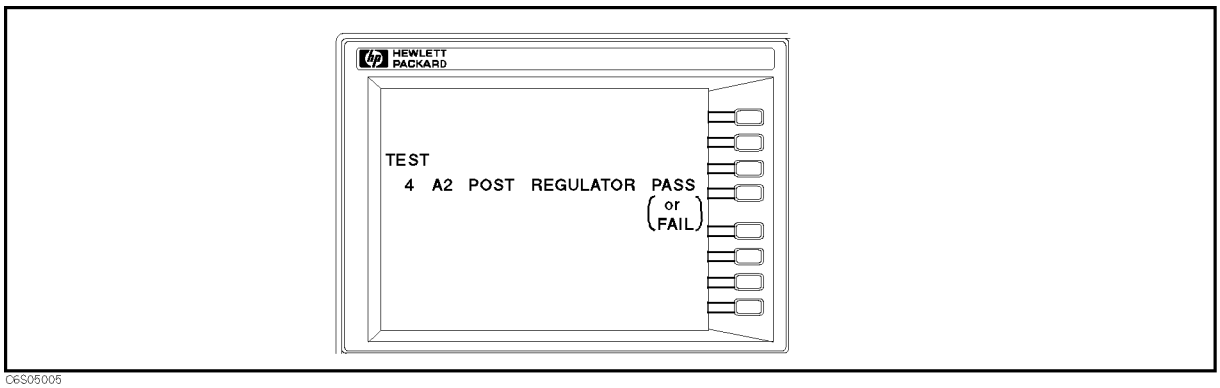

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Figure 5-5. Displayed Test Result

- If "PASS" is displayed, the power supply function group are working properly with a 95% confidence level. To confirm the last 5% uncertainty of the A2 power supplies, measure all A2 power supply voltages. See the *MEASURE A2 POST-REGULATOR OUTPUT VOLTAGE* at the end of this chapter.
- If "FAIL" is displayed, perform the following steps.
  a. Press `RETURN`, `SERVICE MODES`, `BUS MEAS [ON]`, `DC BUS`. Then the abbreviated faulty power supply is displayed on the LCD.
  b. Continue with *TROUBLESHOOT A2 POST-REGULATOR* in this chapter. In particular, check the faulty power supply.

FIND OUT WHY THE FAN IS NOT ROTATING

If the fan is not rotating, the problem may be in the A40 pre-regulator, the A50 DC-DC Converter, the A2 post-regulator, or the fan.

1. Check the Line Voltage, Selector Switch Setting, and Fuse

Check the main power line cord, line fuse, and actual line voltage to see that they are all correct. Figure 5-6 shows how to remove the line fuse, using a small flat-bladed screwdriver to pry off the fuse holder. For more information about the line cord, see the *Power Requirements* in Appendix B.

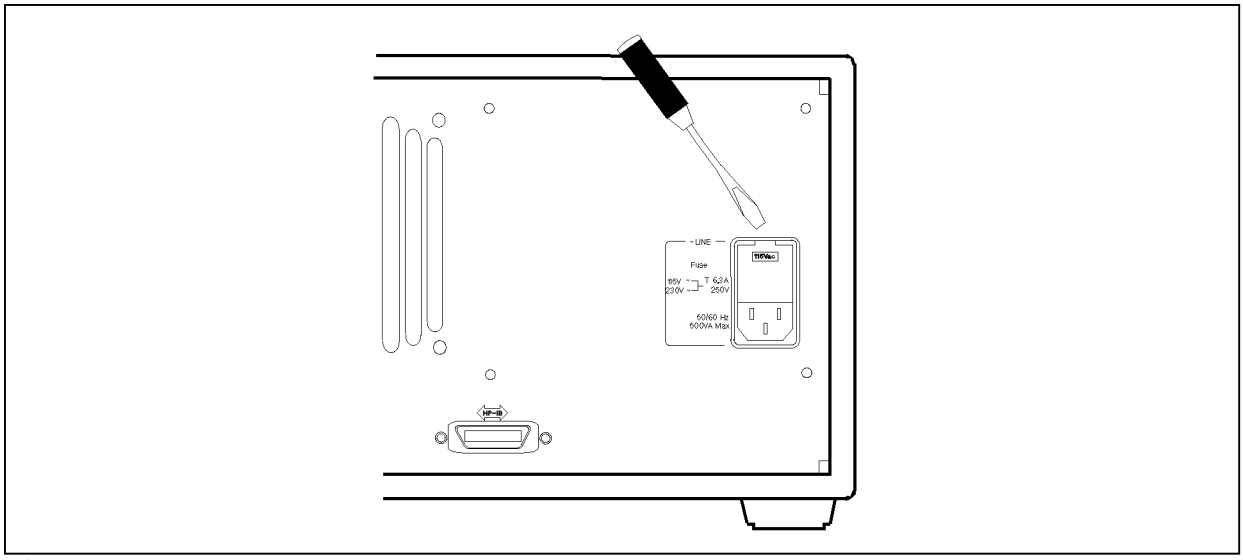

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Figure 5-6. Removing Line Fuse

2. Check the A50 SHUTDOWN LED

When the fan stops, the A50 SHUTDOWN LED is off. See Figure 5-12 Power Supply Block Diagram 1. The fan generates a FAN LOCK signal. The signal is fed into the FAN LOCK SENSE circuit in the A50 DC-DC Converter. If the FAN stops, the FAN LOCK signal is missing. Then the FAN LOCK SENSE circuit activates the A50 SHUTDOWN circuit and turns off the SHUTDOWN LED.

Perform the following procedure to check the A50 SHUTDOWN LED.

a. Remove the analyzer's top cover and shield plate.

b. Make sure the A2 post-regulator is firmly seated and the cables are connected properly.

c. Turn the analyzer power on.

d. Look at the A50 SHUTDOWN LED. The LED location is shown in Figure 5-2.

- If the SHUTDOWN LED is on, replace the A50 DC-DC Converter.
- If the SHUTDOWN LED is off, check the cable connection between A50J2 and A2J4. If the connection is good, continue with *TROUBLESHOOT THE FAN AND THE A50 DC-DC Converter* in this chapter.

FIND OUT WHY THE A50 SHUTDOWN LED IS OFF

Use this procedure when the fan is rotating. If the fan is not rotating, see the *FIND OUT WHY THE FAN IS NOT ROTATING*.

If the fan is rotating, the A50 SHUTDOWN LED turning off indicates the A50 shutdown circuit is protecting the +5 VD power supply from the over voltage condition. The +5 VD power line may be shorted with one of power lines higher than +5 V. The problem may be in the A50 DC-DC Converter, the A2 post-regulator, and any of assemblies obtaining the power from +5 VD supply and the higher power supplies.

1. Disconnect the Cable from the A50J1

Turn the analyzer power off. Disconnect the cable from the A50J1. Turn the analyzer power on.

- If the A50 SHUTDOWN LED is still off, replace the A50 DC-DC Converter.
- If the A50 SHUTDOWN LED goes on, the A50 DC-DC Converter is verified. Turn the analyzer power off and reconnect the cable to the A50J1. Continue with the next *Disconnect the Cable from the A51J2*.

2. Disconnect the Cable from the A51J2

Turn the analyzer power off. Disconnect the cable from the A51J2. Turn the analyzer power on.

- If the A50 SHUTDOWN LED goes on, replace the A51 GSP.
- If the A50 SHUTDOWN LED is still off, the A51 GSP is verified. Turn the analyzer power off and reconnect the cable to the A51J2. Continue with the next *Disconnect the Cable from the A1J10*.

3. Disconnect the Cable from A22J1 (Option 001 Only)

Turn the analyzer power off. Disconnect the cable from A22J1. Turn the analyzer power on.

- If the A50 SHUTDOWN LED goes on, replace the A22 DC Bias 1/2.
- If the A50 SHUTDOWN LED is still off, the A22 DC Bias 1/2 is verified. Turn the analyzer power off and reconnect the cable to A22J1. Continue with *Disconnect the Cable from A1J10*.

4. Disconnect the Cable from the A1J10

Turn the analyzer power off. Disconnect the cable from A1J10. Turn the analyzer power on.

- If the A50 SHUTDOWN LED goes on, replace the A1 CPU.
- If the A50 SHUTDOWN LED is still off, the A1 CPU is verified. Turn the analyzer power off and reconnect the cable to the A1J10. Continue with the next *Remove Assemblies*.

5. Remove Assemblies

a. Turn the analyzer power off.

b. Remove the assemblies, A3, A4, A5, and A6. Don't remove the A2 post-regulator.

c. Turn the analyzer power on.

- If the A50 SHUTDOWN LED is still off, the A2 post-regulator is probably faulty. Replace the A2 post-regulator. If the SHUTDOWN LED is still off after replacing the A2 post-regulator, inspect the A20 motherboard for soldering bridges and shorted traces on the FAN POWER and the FAN LOCK signal paths.
- If the A50 SHUTDOWN LED goes on, the A2 post-regulator and the A20 motherboard are verified. Continue with the next step.

d. Reinstall each assembly one at a time. Turn the analyzer power on after each is installed. The assembly that causes the A50 SHUTDOWN LED to go on is the most probable faulty assembly. Replace the assembly.

FIND OUT WHY THE A1 +5 VD LED IS NOT ON STEADILY

If the +5 VD LED is not on steadily, the +5 VD line voltage is missing or is not steady enough to power the analyzer. The problem may be in the A40 pre-regulator, A50 DC-DC Converter, the A1 CPU, or any of assemblies obtaining power from +5 VD supply.

1. Check the A40 Pre-regulator

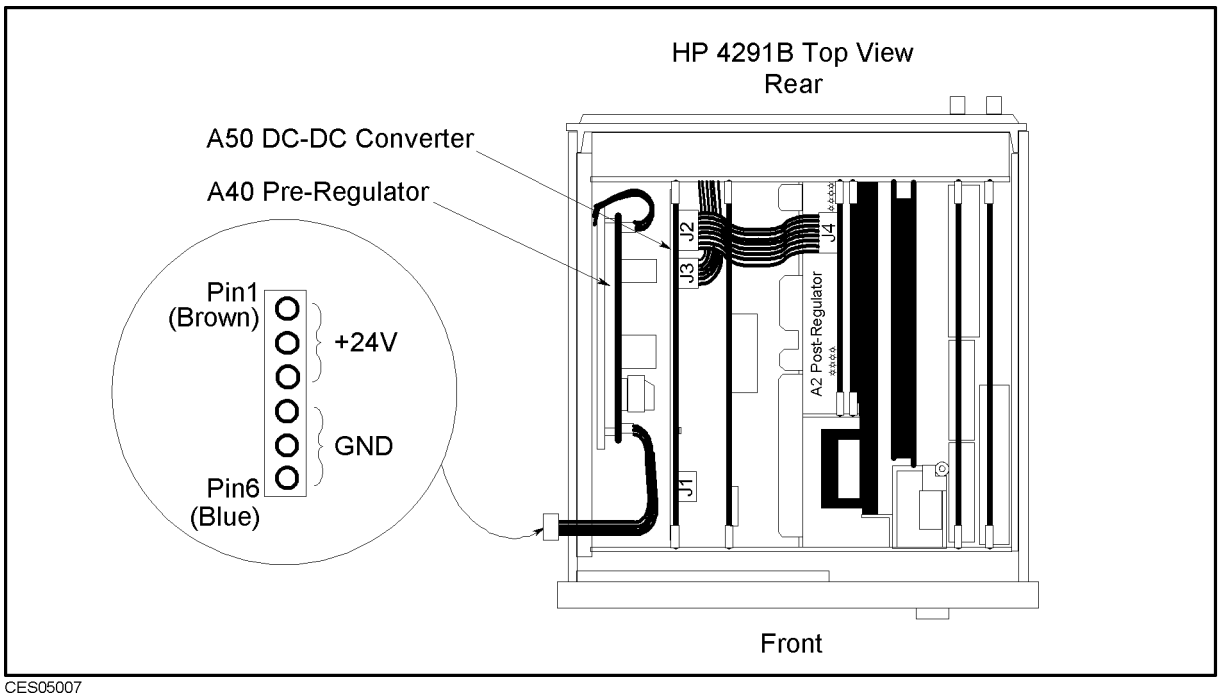
a. Turn the analyzer power off.

b. Disconnect the cable from A40J1. The A40J1 location is shown in Figure 5-7.

c. Turn the analyzer power on.

d. Check the voltage between the pin 1 and pin 6(GND) of the cable within +22.0 V to +27.0 V using a voltmeter with a small probe.

- If the voltmeter reading is out of the limits, replace the A40 pre-regulator.
- If the voltmeter reading is within the limits, the A40 pre-regulator is verified. Turn the analyzer power off and reconnect the cable to the A50J1. Then continue with the next *Check the A50 DC-DC Converter* section.



CES05007

Figure 5-7. A40J1 Output Voltage

2. Check the A50 DC-DC Converter

a. Turn the analyzer power off.

b. Disconnect a cable form the A50J3. The A50J3 location is shown in Figure 5-7.

c. Turn the analyzer power on.

d. Check the voltage between the A50J3 pin 1 and pin 6(GND) within +4.59 V to +5.61 V using a voltmeter with a small probe.

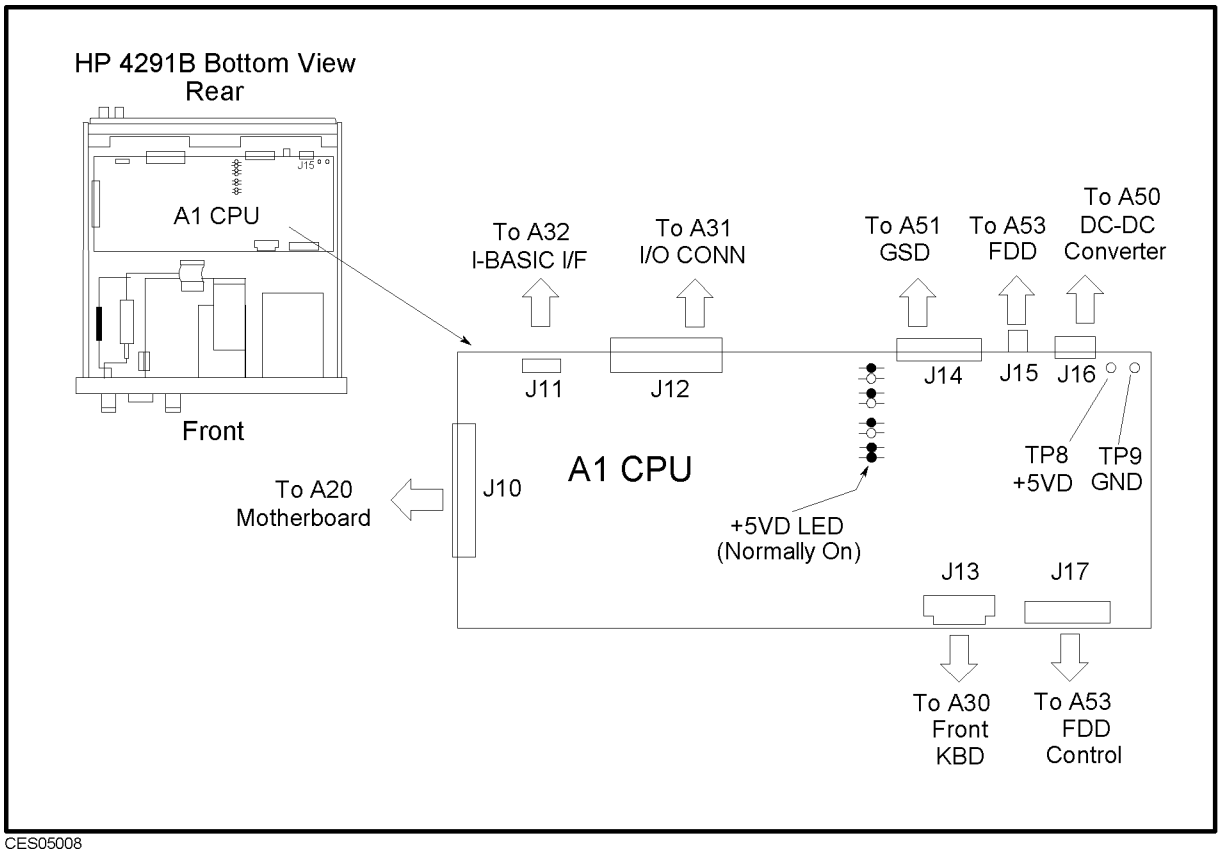
- If the voltmeter reading is out of the limits, replace the A50 DC-DC Converter.

- If the voltmeter reading is within the limits, the A50 +5 VD power supply is verified. Turn the analyzer power off and reconnect the cable to the A50J3. Then continue with the next *Disconnect Cables on the A1 CPU* section.

3. Disconnect Cables on the A1 CPU

a. Turn the analyzer power off.

b. Disconnect cables from the A1 CPU's connectors, J10, J11 (if option 1C2 installed), J12, J13, J14, J16, and J17. The connector locations are shown in Figure 5-8



CES05008

Figure 5-8. A1 CPU Connector Locations

c. Turn the analyzer power on. Look at the A1 +5 VD LED.

- If the LED is still off, the A1 CPU is probably faulty. Replace the A1 CPU.
- If the LED goes on, the A1 CPU is verified. Continue with the next step.

d. Turn the analyzer power off. Reconnect the cable to A1J10. Turn the analyzer power on. Look at the A1 +5 VD LED.

- If the +5 VD LED goes out, the problem may be in the analog assemblies. Continue with *Remove Assemblies*.
- If the + 5 VD LED is still on, continue with the next step.

e. Reconnect one of the disconnected cables to its connector at a time. Turn the analyzer power on after each cable is connected. The assembly related with the cable turning the +5 VD LED off is probably faulty. Replace the assembly.

4. Remove Assemblies

a. Turn the analyzer power off. Remove the A3, A4, A5, and A6 assemblies. Do not remove the A2 post-regulator.

b. Turn the analyzer power on. Look at the A1 +5 VD LED.

- If the LED is still off, replace the A2 post-regulator. If the +5 VD LED is still off after replacing the A2 post-regulator, inspect the A20 motherboard for soldering bridges and shorted traces on the +5 VD power line.
- If the LED goes on, the A2 post-regulator and the A20 motherboard are verified. Continue with the next step.

c. Reinstall one of the removed assemblies at a time. Turn the analyzer power on after each is installed. The assembly that turns the A1 +5 VD LED on is the most probable faulty assembly. Replace the assembly.

TROUBLESHOOT THE FAN AND THE A50 DC-DC CONVERTER

Perform the following procedure to troubleshoot the fan and the A50 DC-DC Converter.

1. Troubleshoot the Fan

a. Turn the analyzer power off.

b. Disassemble the rear panel.

c. Remove the fan power cable from the Motherboard A20J18.

d. Connect a DC power supply, a 10 kΩ resistance, and a oscilloscope to the fan power cable using appropriate wires as shown in Figure 5-9.

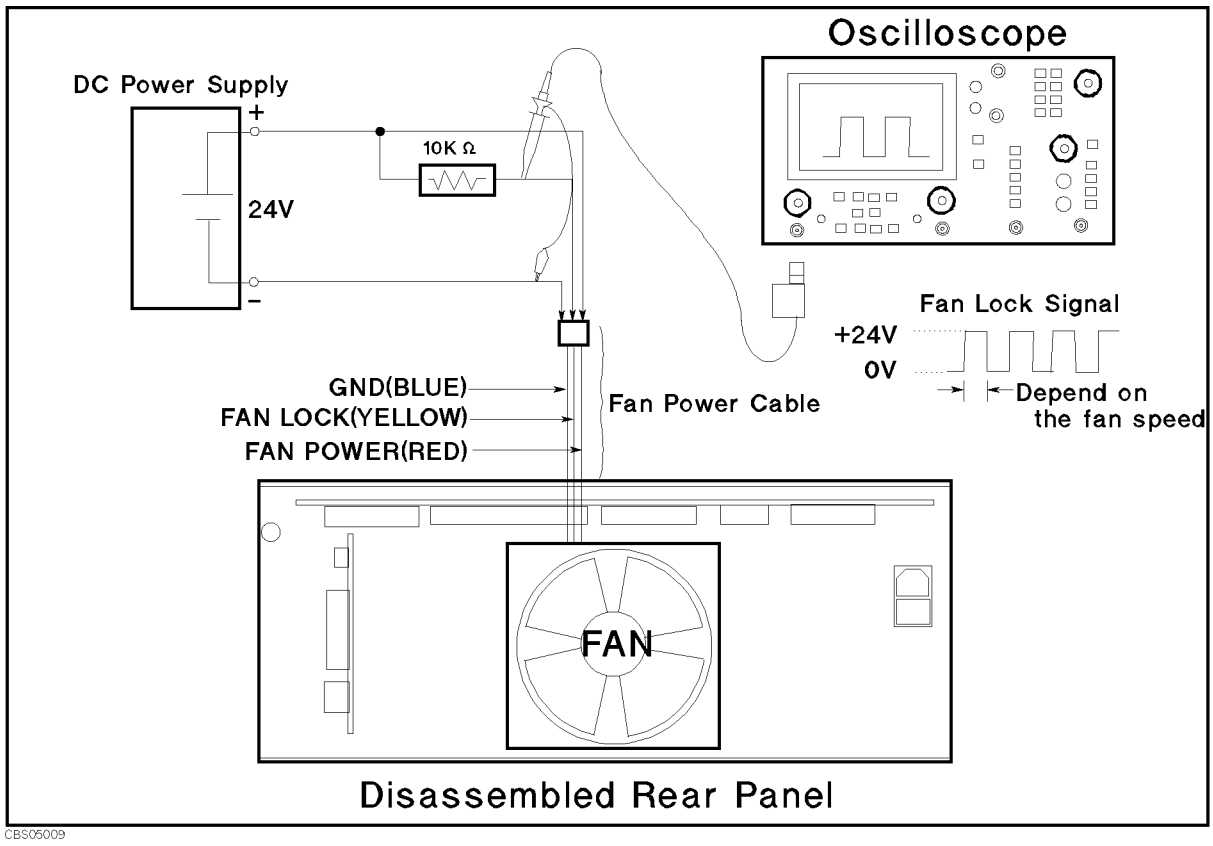


Figure 5-9. Fan Troubleshooting Setup

e. Turn the DC power supply on. Adjust the output voltage to +24 V.

f. Check the fan is rotating. Check the FAN LOCK signal is as shown in Figure 5-9.

- If the fan is not rotating or the FAN LOCK signal is unexpected, replace the fan.
- If these are good, the fan is verified.
- Reconnect the fan power cable to the Motherboard A20J18.

2. Troubleshoot the A50 DC-DC Converter

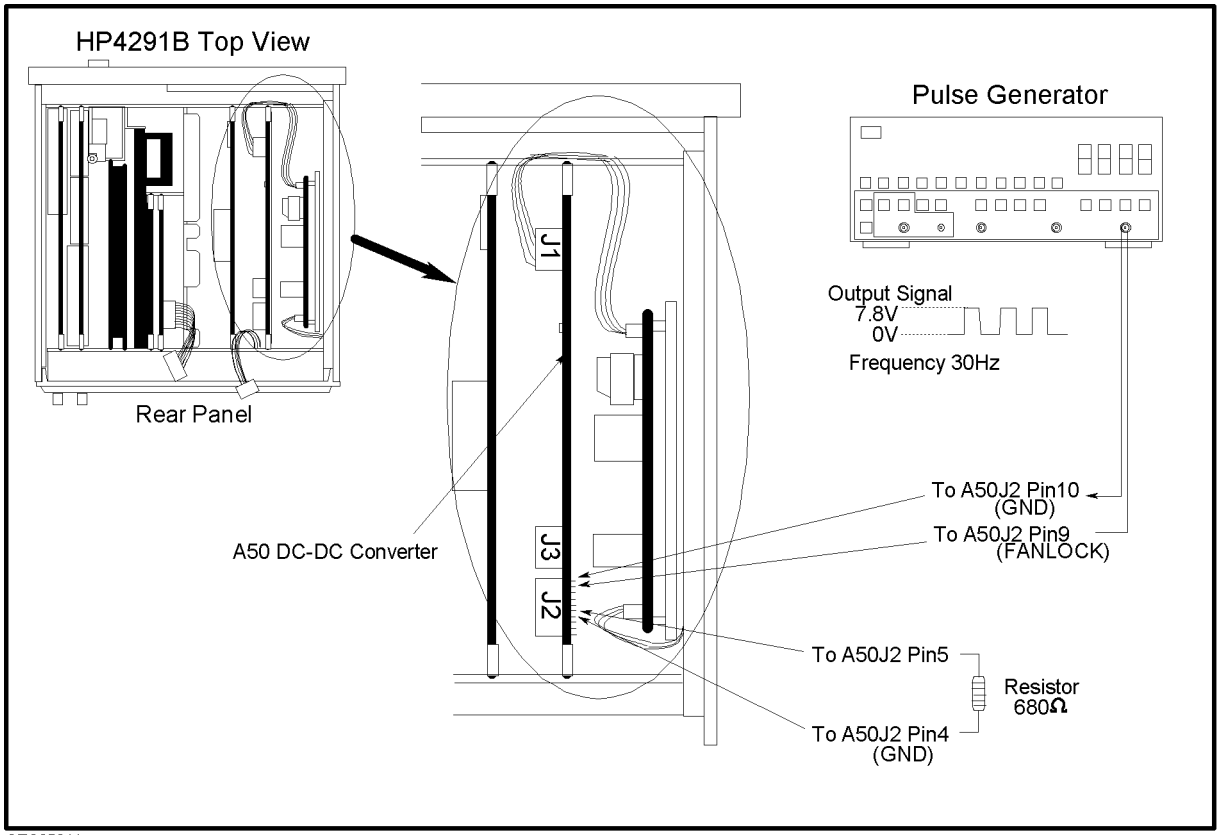


Figure 5-10. A50 DC-DC Converter Troubleshooting Setup

a. Turn the analyzer power off.

b. Disconnect cables from the A50J2 and A50J3. The connector locations are shown in Figure 5-10

c. Connect the pulse generator to the A50J2 as shown in Figure 5-10. The pulse generator is used to feed the substitute of the FAN LOCK signal to the A50 DC-DC converter. This purposes not to shut down the A50 DC-DC converter.

d. Turn the pulse generator power on. Set the controls as follows:

Wave Form	Square
Frequency	Approximately 30 Hz
Amplitude	+7.8 V

e. Connect a resister (approximately 680ohms, 125mW) between the A50J2 pin 5 (+7.8 V) and pin 4(GND) as shown in Figure 5-10.

f. Turn the analyzer power on.

g. Measure all power supply voltages on A50J2 and A50J3 using a voltmeter with a small probe. See the Table 5-1 for power lines, connector pins, and limits.

Table 5-1. A50 Power Supplies

Supply	Connector Pin	GND Connector Pin	Range
+5 VD	A50J3 Pin 1, 2, and 3	A50J3 Pin 4, 5, and 6	+4.6 V to +5.7 V
-18 V	A50J2 Pin 1	A50J2 Pin 3 and 4	-14.0 V to -27.0 V
+18 V	A50J2 Pin 2	A50J2 Pin 3 and 4	14.0 V to 27.0 V
+7.8 V	A50J2 Pin 5	A50J2 Pin 3 and 4	7.0 V to 9.0 V
-7.8 V	A50J2 Pin 6	A50J2 Pin 3 and 4	-6.0 V to -12.0 V
+24 V	A50J2 Pin 8	A50J2 Pin 10	22.0 V to 27.0 V

- If any of the power supply voltages are out of the limits, replace the A50 DC-DC Converter.
- If all A50 power supply voltages are good, the A50 pre-regulator is verified.

TROUBLESHOOT THE A2 POST-REGULATOR

Use this procedure when the fan is rotating and the A50 SHUTDOWN LED turns on.

If one or some of the A2 eight LEDs are not on steadily, the corresponding A2 power supply voltages, -15 V, -5 V, +5 V, +5.3 V, +15 VD, are missing or are not enough to power the analyzer. The problem may be in the A40 pre-regulator, the A50 DC-DC Converter, the A2 post-regulator, and any of assemblies obtaining the A2 post-regulator.

1. Check the A40 Pre-Regulator

See *FIND OUT WHY THE A1 +5VD LED IS NOT ON STEADILY* section to verify the A40 Pre-Regulator.

2. Check the A50 DC-DC Converter

See *TROUBLESHOOT THE FAN AND THE A50 DC-DC CONVERTER* section to verify the A50 DC-DC Converter.

3. Remove Assemblies

See *FIND OUT WHY THE A1 +5VD LED IS NOT ON STEADILY* section to verify the A3, A4, A5, A6 and A60.

4. Measure the A2 Post Regulator Output Voltages

Use this procedure to measure all A2 post-regulator voltages. If all A2 output voltages are within the limits, the A2 post-regulator is verified with 100% confidence.

This procedure put out the A2 post-regulator from the analyzer and measure the voltages on the A2J3 pins. A pulse generator is used to feed the substitute of the FAN LOCK signal to the A2 post regulator. This purposes not to shut down the A50 DC-DC converter.

a. Turn the analyzer power off.

b. Remove the cable from A2J4.

c. Remove A2 post-regulator from the analyzer.

d. Reconnect the cable between the A2J4 and the A50J2 as shown in Figure 5-11.

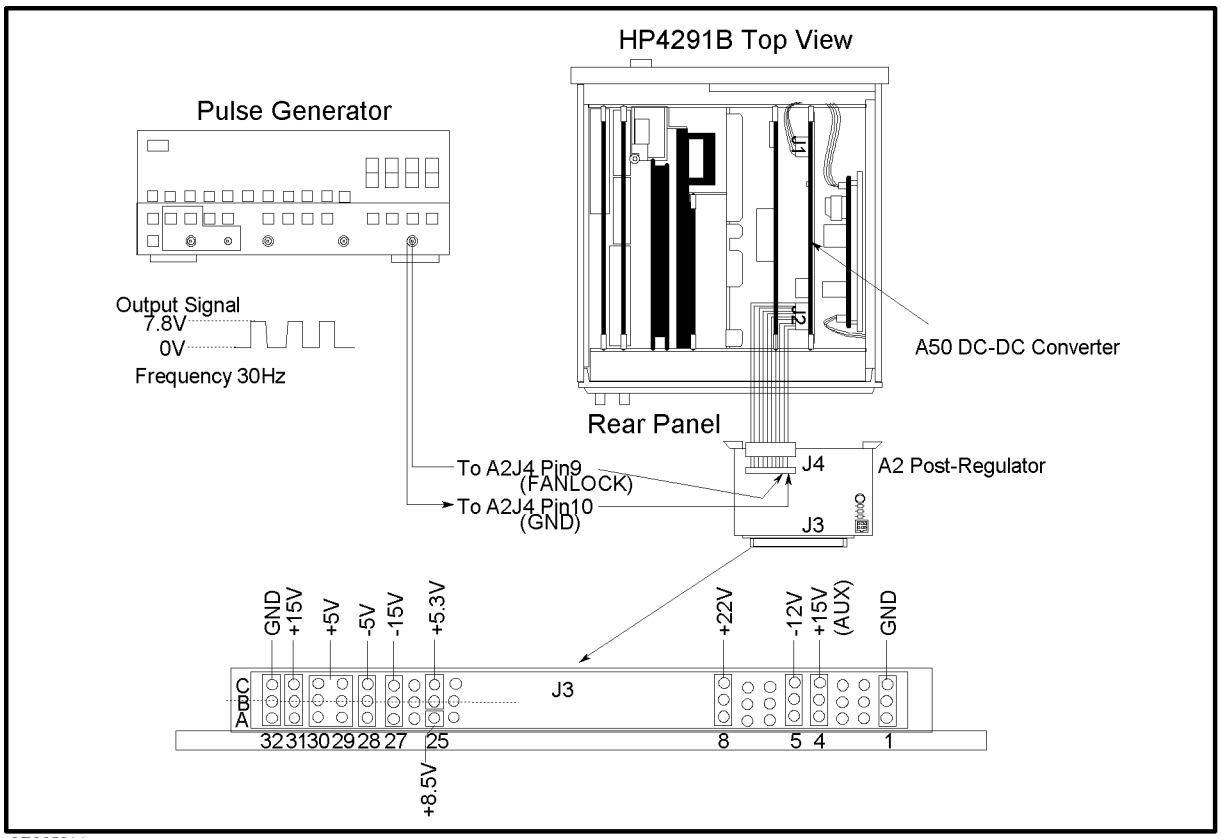


Figure 5-11. A2 Output Voltage Measurement Setup

e. Connect the pulse generator to the A2J4 as shown in Figure 5-11.

f. Turn the pulse generator power on. Set the controls as follows:

Wave Form	Square
Frequency	Approximately 30 Hz
Amplitude	+7.8 V

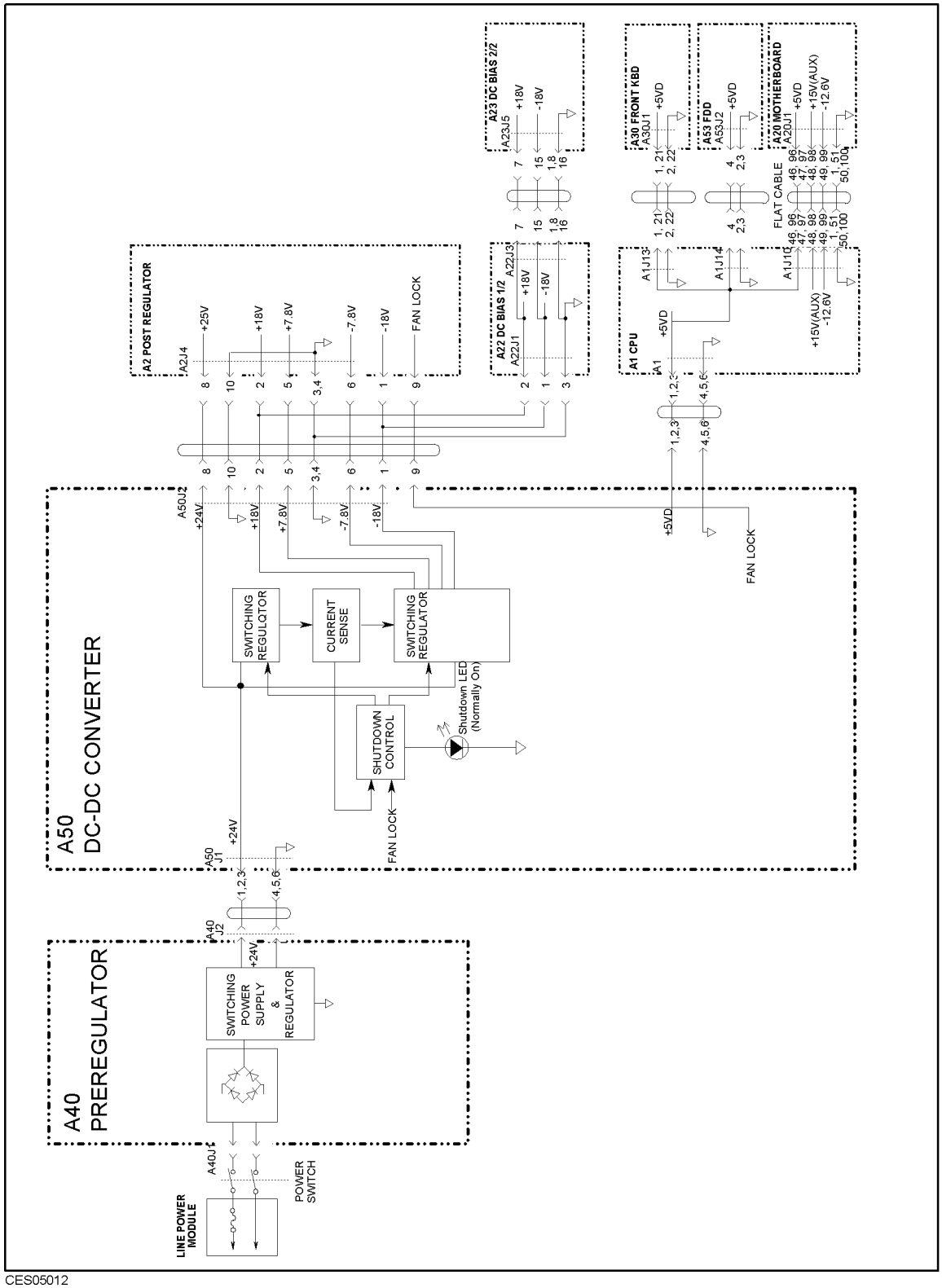
g. Turn the analyzer power on.

h. Measure the A2 output voltages at the A2J3 pins using a voltmeter with a small probe. See Figure 5-11 and Table 5-2 for the power supplies, A2J3, and the limits.

Table 5-2. Power Supplies on A2 Post-Regulator

Supply	Connector Pin	Range
+22 V	J3 Pin 8	19.8 V to 24.2 V
+15 V(AUX)	J3 Pin 4	13.5 V to 16.5 V
+15 V	J3 Pin 31	13.5 V to 16.5 V
+8.5 V	J3 Pin 25C	7.65 V to 9.35 V
+5.3 V	J3 Pin 25A 25B	4.77 V to 5.83 V
+5 V	J3 Pin 30 29	4.5 V to 5.5 V
-5 V	J3 Pin 28	-4.5 V to -5.5 V
-12 V	J3 Pin 5	-10.8 V to -13.2 V
-15 V	J3 Pin 27	-13.5 V to -16.5 V
FAN POWER	J3 Pin 8	19.2 V to 28.8 V
GND	J3 Pin 3,4,10	
	J5 Pin 4	

- If any of the line voltages are out of the limits, replace the A2 post-regulator.
- If all line voltages are within the limits, the A2 post-regulator is verified.



CES05012

Figure 5-12. Power Supply Block Diagram 1

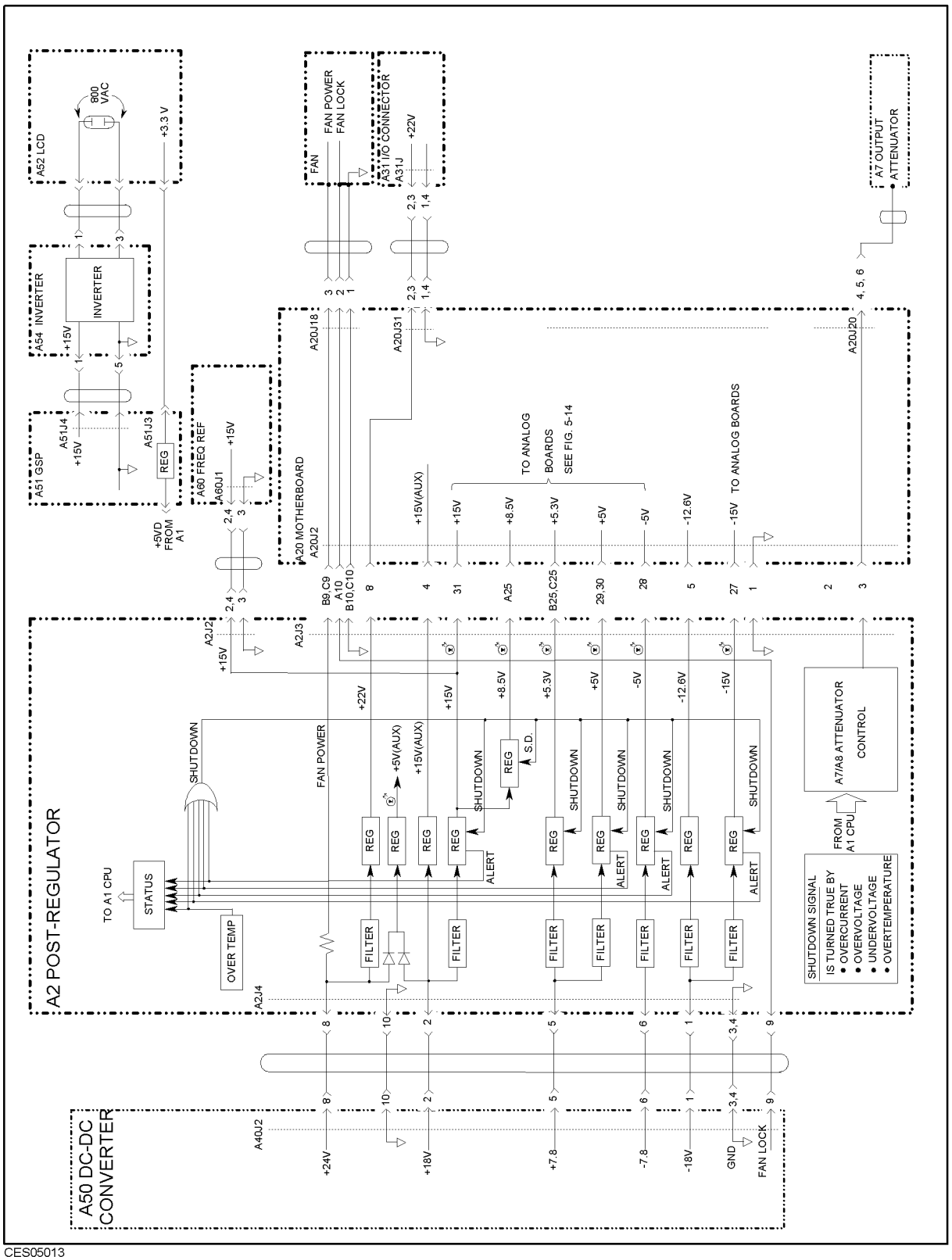


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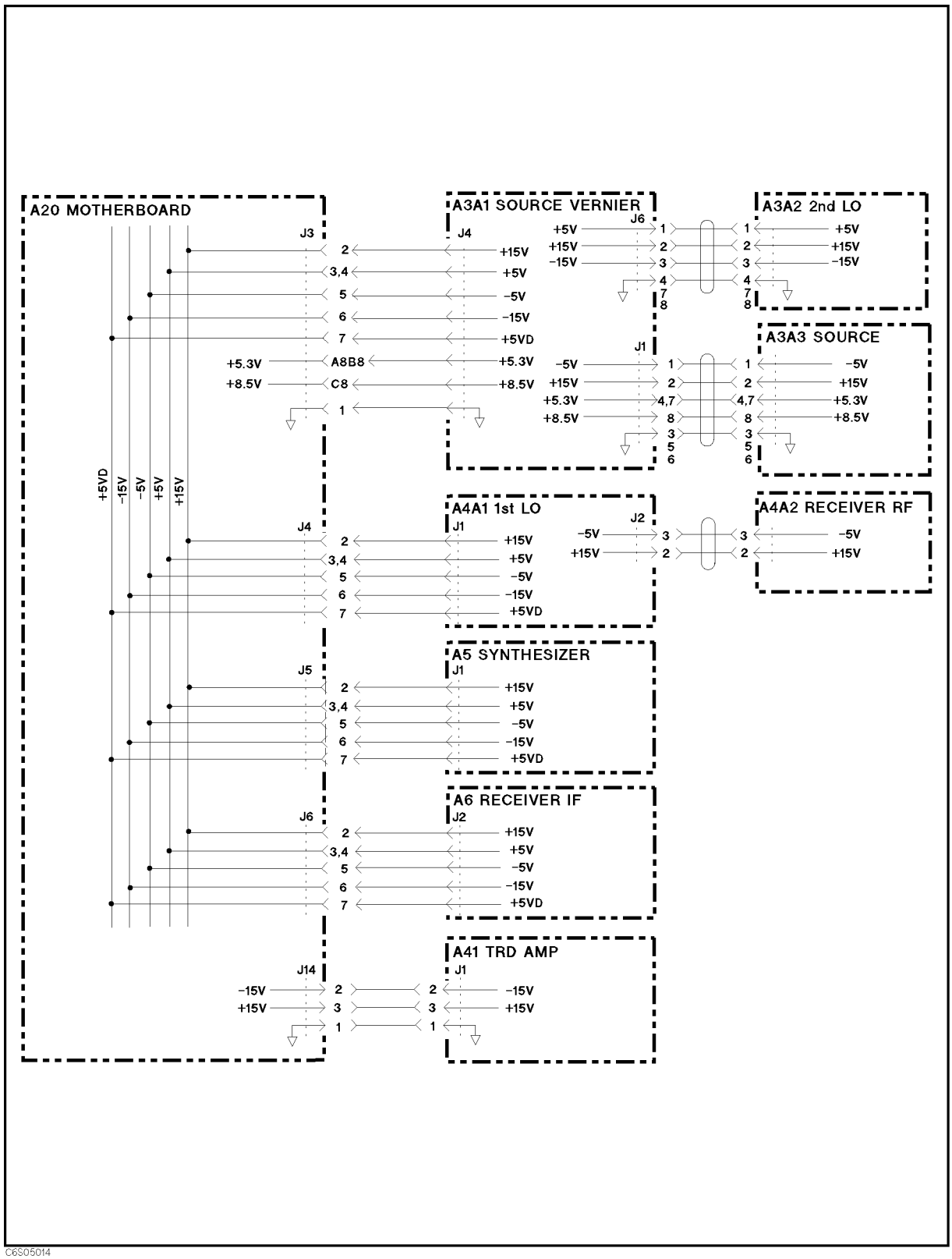
Figure 5-13. Power Supply Block Diagram 2



C6S05014

Figure 5-14. Power Supply Block Diagram 3

6

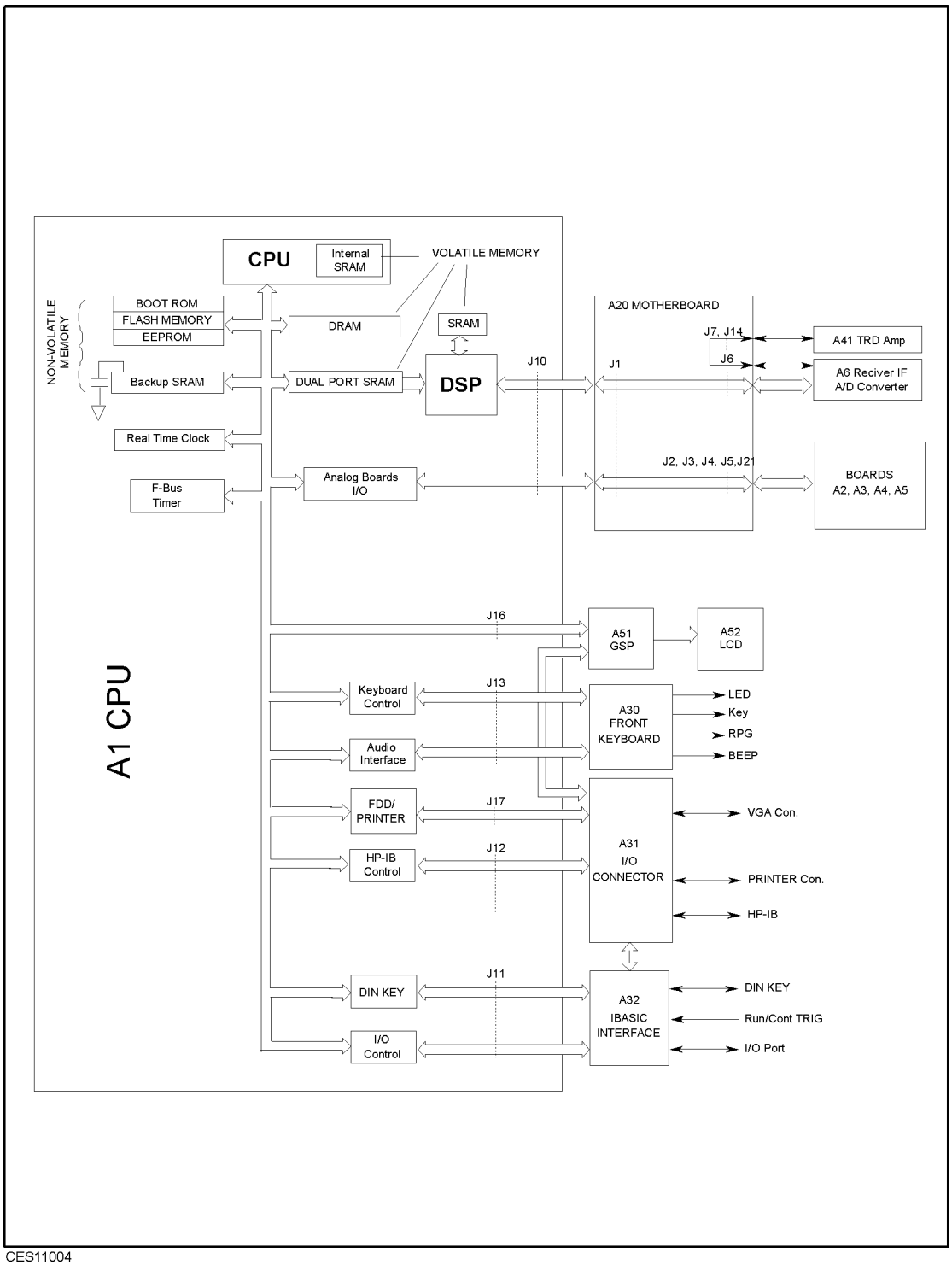
Digital Control Troubleshooting

INTRODUCTION

Use this procedure only if you have followed the procedures in the *Troubleshooting* chapter, and believe the problem to be in the digital control group. This procedure is designed to let you identify the bad assembly within the digital control group in the shortest possible time. Whenever an assembly is replaced in this procedure, refer to the *Table of Related Service Procedures* in the *Post-Repair Procedures* chapter in this manual.

Figure 6-1 shows the digital control group in simplified block diagram form. The following assemblies make up the digital control group:

- A1 CPU
- A30 Front Keyboard
- A31 I/O Connector
- A32 I-BASIC Interface
- A51 GSP
- A52 LCD(Liquid Crystal Display)
- A53 FDD



CES11004

Figure 6-1. Digital Control Group Simplified Block Diagram

START HERE

1. Check the Power On Sequence

See the INSPECT THE POWER ON SEQUENCE in the chapter 3 for checking the Power On Sequence.

Check the Ch 1 and Ch 2 Operations

a. Press Ch 1 and Ch 2 alternately.

b. Check that the two LEDs alternately light each time you press the keys.

- If both LEDs would not light, continue with the next *Check the A1 Eight LEDs*.
- If the two LEDs do not alternately light (the Ch 1 LED is still lit even if pressing the Ch 2), the A1 CPU is probably faulty. Replace the A1 CPU.
- If the two LEDs alternately light each time you press the keys, the A1 CPU is probably working properly. Continue with the *TROUBLESHOOT THE A51 GSP AND A52 LCD* in this chapter.

Check the A1 Eight LEDs

There are eight LEDs on the A1 CPU. These LEDs should be in the pattern shown in Figure 6-2 at the end of the power on sequence. Perform the following procedure to check the A1 eight LEDs.

a. Turn the analyzer turn off.

b. Remove the bottom cover of the analyzer.

c. Turn the analyzer power on.

d. Look at the A1 eight LEDs. Some of the LEDs light during the power on sequence. At the end of the power on sequence, the LEDs should stay in the pattern shown in Figure 6-2. If the LEDs stay in the other pattern, the A1 CPU is probably faulty. Replace the A1 CPU.

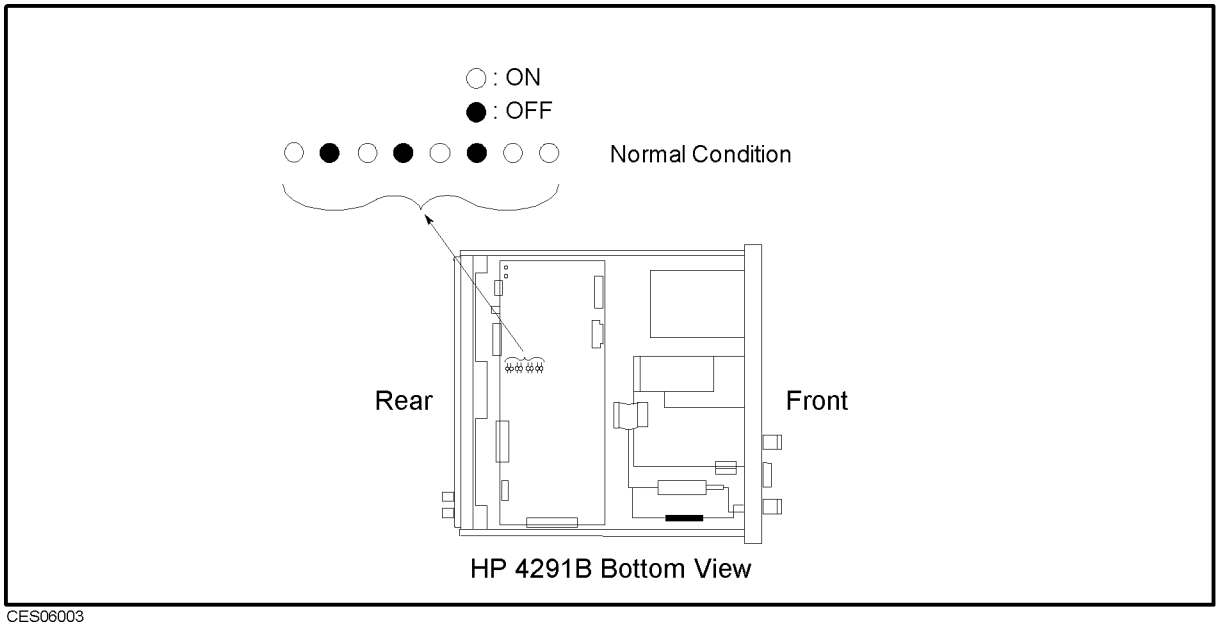


Figure 6-2. A1 Eight LEDs' Pattern

2. Check Error Messages

Turn the analyzer power on. Check no error message appears on the LCD.

- If no error message is displayed, continue with the *Check A1 DRAM and Flash Memory* in this *START HERE*.
- If one of error messages listed below is displayed, follow the instruction described below. For the other message, see the *Error Messages* in Messages.

Error Messages	Instruction
POWER ON TEST FAILED	This indicates the power on selftest failed. Continue with the next *Check Power On Selftest*.
EEPROM CHECK SUM ERROR	This indicates that the correction constants stored in the EEPROM on the A1 CPU are invalid or the EEPROM is faulty. Rewrite all correction constants into the EEPROM. For the detailed procedure, See the *Adjustments and Correction Constants* chapter in this manual. If the rewriting is not successfully performed, replace the EEPROM and then rewrite the all correction constants into the new EEPROM.
Svc (Status Annotation)	This indicates that the correction constants stored in the EEPROM on the A1 CPU are invalid or the EEPROM is faulty. See the instruction of the EEPROM CHECK SUM ERROR message.
POWER FAILED ON - - -	One or some of A2 power supplies, +15 V, +8.5 V, +5.3 V, +5 V, -5 V, -15 V are displayed in - - - of the message. The displayed power supplies are shut down due to the trouble on the A2 post-regulator. Continue with the *Power Supply Troubleshooting* chapter.
POWER FAILED ON PostRegHot	This indicates A2 power supplies, +15 V, +8.5 V, +5.3 V, +5 V, -5 V, -15 V, are shut down due to too hot heat sink on A2 post-regulator. Cool down the analyzer for about 30 minutes. Then turn the analyzer power on. If this message is still displayed, replace A2 post-regulator.
PHASE LOCK LOOP UNLOCKED	This indicates one or some of PLLs (phase lock loops) in the oscillators listed below is not working properly. These oscillators are checked in the internal test 0: ALL INT. Continue with the next *Check the Power On Selftest* in where the ALL INT test is executed.

Identify the First Failed Test

If the power on selftest fails and "POWER ON TEST FAILED" message is displayed, execute the ALL INT test to identify the first failed test, using the following procedure. If internal test 1: A1CPU is the first failed test, replace A1 CPU. Otherwise, see Chapter 4.

a. Press (PRESET), (SYSTEM), SERVICE MENU, TESTS, (0), and (x1) to access the internal test 0: ALL INT.

b. Press EXECUTE TEST to execute the ALL INT test.

c. Wait until the test result, PASS or FAIL, is displayed.

d. Press the (⇧), (⇩) keys to find the first occurrence of a FAIL message for tests 1 and 4 through 16.

3. Check the A1 DRAM and Flash Memory

The A1 DRAM and flash memory are tested on the sequence to access the bootloader menu. For the bootloader menu, see the *Service Key Menus* chapter.

Perform the following procedure to verify the A1 DRAM and flash memory.

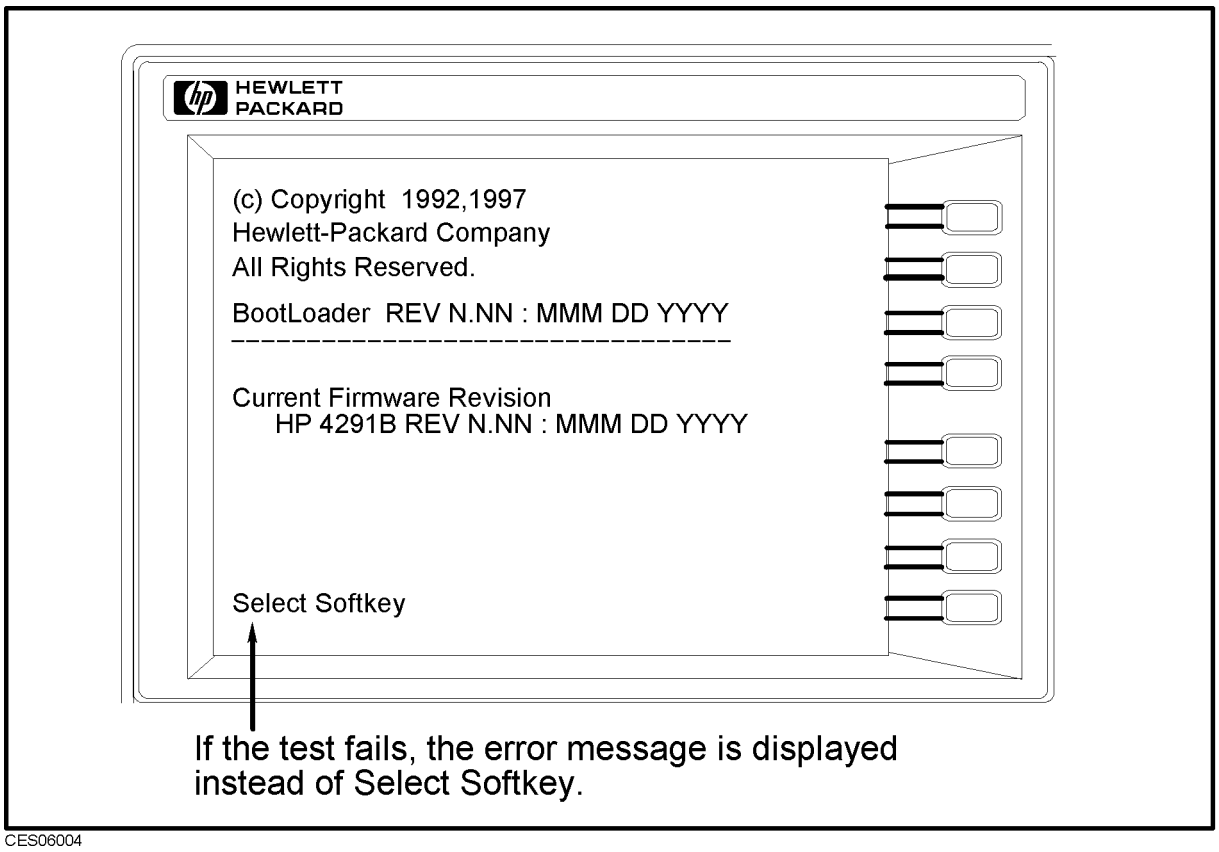
a. Turn the analyzer power off.

b. Push two keys (Start) and (Preset). With keeping the two keys pushed down, turn the analyzer power on.

c. Wait for the display shown in Figure 6-3 appears on the LCD.

d. Check no error message displayed on the LCD.

- If no error message is displayed, the A1 DRAM and flash memories are verified. Continue with the next *Check the A1 Volatile Memory* .
- If an error message is displayed or the display shown in Figure 6-3 does not appear, the A1 CPU is probably faulty. Replace the A1 CPU.



CES06004

Figure 6-3. Bootloader Display

4. Check the A1 Volatile Memory

a. Turn the analyzer power on.

b. Press (System), SERVICE MENU, TESTS, (2), (x1), EXECUTE TEST to run the internal test 2: A1 VOLATILE MEMORY.

c. Check no error message displayed. At the end of this test, the analyzer returns the control settings to the default values (power on reset). If the test fails, the analyzer displays an error messages for a few second before returning to the defaults.

- If no error message is displayed, the A1 volatile memories are verified. Continue with the next *Check the A30 Front Keyboard*.
- If one of error messages listed below is displayed, the A1 CPU is faulty. Replace the A1 CPU.

```
CPU INTERNAL SRAM R/W ERROR
DSP SRAM R/W ERROR
DUAL PORT SRAM R/W ERROR
CPU BACKUP SRAM R/W ERROR
```

5. Check the A30 Front Keyboard

The A30 front keyboard can be checked using the external test 17: FRONT PANEL DIAG.

a. Press (PRESET), (SYSTEM), SERVICE MENU, TESTS, (1), (7), (x1), EXECUTE TEST to run the external test 17.

b. Press all of the front panel keys. The pressed abbreviated key name should be displayed at a key pressed. When you rotate the RPG knob, the RPG tuned direction (CW or CCW) and its response speed (SLOW, MID, FAST) should be displayed. So you can check every key on the A30 Keyboard except for (PRESET). (If you want to exit this test, press (PRESET).)

- If one or more keys seems to be defective, replace the A30 front keyboard.
- If all keys seem to be good, the A30 front keyboard is verified. Continue with the next *Check the A53 FDD*.

6. Check the A53 FDD

The A53 FDD (Flexible Disk Drive) can be checked using the external test 18: DISK DR FAULT ISOL'N.

a. Press (PRESET), (SYSTEM), SERVICE MENU, TESTS, (1), (8), (x1), EXECUTE TEST to run the external test 18.

b. As the analyzer instructs, insert a flexible disk into FDD. Use a formatted but blank flexible disk, otherwise the data on the disk will be overwritten by this test. Then press CONT.

c. Check the test result, PASS or FAIL, that is displayed at the end of the test.

- If this test fails, replace the A53 FDD.

7. Check the A32 I-BASIC Interface and the mini DIN Keyboard

The mini DIN external keyboard is connected to the A32 I-BASIC I/O connector, and is used to develop programs.

If the external keyboard of the I-Basic is not working, perform the following procedure to verify the keyboard.

Press (PRESET), (SYSTEM), SERVICE MENU, TESTS, (1), (x1), EXECUTE TEST to run the internal test 1: A1 CPU.

- If the internal test 1 passes, the HP HIL driver circuit on the A1 CPU is probably working. Inspect cables between the external keyboard and the A1 CPU through the A32 I-BASIC interface. If the cable is good, replace the external keyboard.
- If the internal test 1 fails, replace the A1 CPU.

TROUBLESHOOT THE A51 GSP and A52 LCD

Use this procedure when the LCD(Liquid Crystal Display) is unacceptable, or not being bright.

1. Run the Internal Test 3: A51 GSP

The A51 GSP can be checked using the internal test 3: A51 GSP. If the test fails, the [Ch 1] and [Ch 2] LEDs blink several time and a few beeps sound at the end of the test. Then the analyzer returns the control settings to the power-on default setting values.

a. Press [PRESET], [SYSTEM], SERVICE MENU, TESTS, [3], [x1], EXECUTE TEST to run the internal test 3. When this test starts, [Ch 1] LED and [Ch 2] LED are turned off.

b. Check the [Ch 1] and [Ch 2] LEDs and the beeps at the end of the test.

- If no beep sound and the LEDs don't blink, the A51 GSP is probably working. Continue with the next *Check the Two LEDs on A51 GSP.*
- If a beep sounds and the LEDs blink one time, the A51 GSP chip is faulty. Replace the A51 GSP.
- If two beep sound and the LED blinks two time, the A51 GSP's DRAM is faulty. Replace the A51 GSP.
- If three beep sound and the LED blinks three time, the A51 GSP's VRAM is faulty. Replace the A51 GSP.

2. Check the A52 LCD(Liquid Crystal Display)

The A52 LCD can be tested using the internal test 40 to 44.

a. Press [PRESET], [SYSTEM], SERVICE MENU, TESTS, [4], [0], [x1], EXECUTE TEST CONTINUE to run the internal test 40, and run the other tests with the same manner.

b. If any defects on the LCD, replace the LCD.

c. If no correct patterns are displayed, check the A54 Inverter.

7

Source Troubleshooting

INTRODUCTION

Use these procedures only if you have read Chapter 4 and you believe the problem is in the source group.

This procedure is designed to let you identify the bad assembly within the source group in the shortest possible time. Whenever an assembly is replaced in this procedure, refer to Chapter 14.

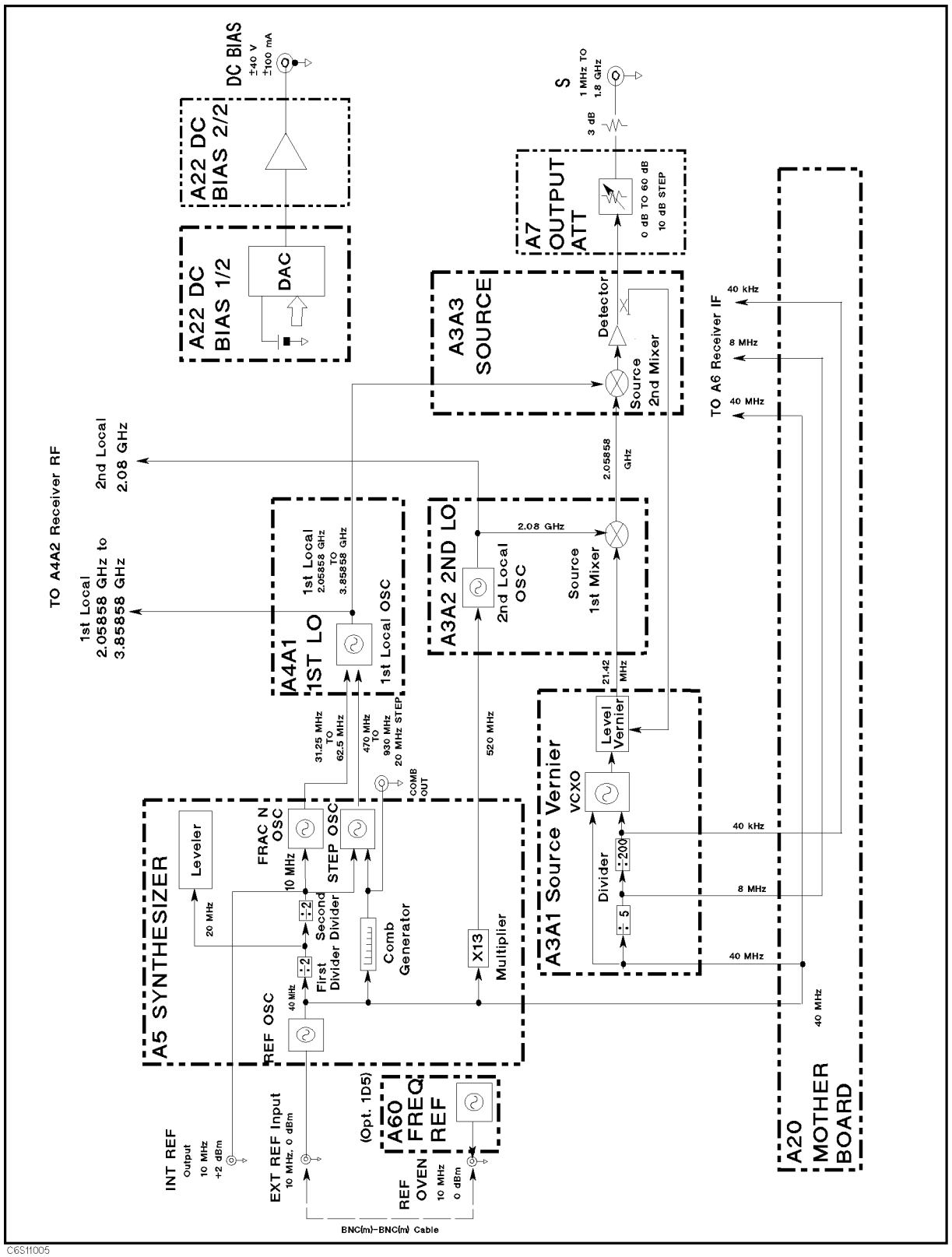
Figure 7-1 shows a simplified block diagram of the source group. The source group consists of the following assemblies:

- A5 Synthesizer
- A4A1 1st LO
- A3A1 Source Vernier
- A3A2 2nd LO
- A3A3 Source
- A7 Output Attenuator
- A22 DC Bias 1/2
- A23 DC Bias 2/2
- A60 High Stability Frequency Reference (Option 1D5)

Note

Make sure all of the assemblies listed above are firmly seated before performing the procedures in this chapter.

Allow the analyzer to warm up for at least 30 minutes before you perform any procedure in this chapter.



C6S11005

Figure 7-1. Source Group Block Diagram

SOURCE GROUP TROUBLESHOOTING SUMMARY

This overview summarizes the sequence of checks included in this chapter. Experienced technicians may save time by following this summary instead of reading the entire procedure. Headings in this summary match the headings in the procedure.

Start Here

1. Run internal test 11. If the test fails, check the INT REF signal. If the INT REF signal is good, replace the A3A1 Source Vernier. If the INT REF signal is bad, replace the A5 Synthesizer.
2. Run internal test 5. If the test fails, replace the A6 Receiver IF in the receiver group.
3. Run internal test 6. If the test fails, replace A5.
4. Run internal test 7. If the test fails, replace A5.
5. Run internal test 8. If the test fails, replace A5.
6. Run internal test 9. If the test fails, replace the A4 1st LO/Receiver RF.
7. Run internal test 13. If the test fails, replace the A3A1 Source Vernier.
8. Run internal test 10. If this test fails, replace the A3A2 2nd LO.
9. Run external test 21. If this test fails, check the A7 Output Attenuator control signals in accordance with the *Check A7 Output Attenuator Control Signals* section in this chapter. If the control signals are good, replace A7. If they are bad, replace the A2 post-regulator.

Check A5 Synthesizer Outputs

1. Check the INT REF signal. If it is bad, replace A5.
2. Check the FRAC N OSC signal. If it is bad, replace A5.
3. Check the STEP OSC signal. If it is bad, replace A5.
4. Check the 520 MHz signal. If it is bad, replace A5.
5. Check the EXT REF operation. If it is bad, replace A5.

Check A4A1 1st LO Outputs

1. Check the 1st local oscillator signal at A4A1J3. If it is bad, replace A4.
2. Check the 1st local oscillator signal at A4A1J4. If it is bad, replace A4.

Check an A3A1 Source Vernier Output

1. Check the 21.42 MHz signal. If it is bad, replace A3A1.

Check A3A2 2nd LO Outputs

1. Check the 2nd local oscillator signal. If it is bad, replace A3A2.
2. Check the 2.05858 GHz signal. If it is bad, replace A3A2.

Check A3A3 Source Output

1. Check the A3A3 RF signal. If it is bad, replace A3A3.

Check A7 Output Attenuator Control Signals

1. Check the A7 control signals. If the control signals are good, replace A7. If the control signals are bad, replace A2.

Check A22 DC Bias 1/2 Output

1. Check the A22 output signals. If the signals are bad, replace A22. Otherwise, replace A23.

Check A60 High Stability Frequency Reference (Option 1D5)

1. Check the REF OVEN signal. If it is bad, replace A60.
2. Perform the *10 MHz Reference Oscillator Frequency Adjustment*. If the adjustment fails, replace A60.

START HERE

The following procedure verifies the operation of each assembly in the source group by using the HP 4291B's self-test functions (internal and external tests). For detailed information about the self-test functions, see the *Service Key Menus*.

In this procedure, the A3A1's divider and the A6's A/D converter (receiver group) are verified first. This is done because the internal tests use the A/D converter to measure voltages at DC bus nodes within the source group. Also, the A3A1's divider output is used to generate the A/D converter's control signals.

Perform the following steps to troubleshoot the source group:

1. Press (Preset), (System), SERVICE MENUS, TESTS, 1, 1, (x1), EXECUTE TEST to run internal test 11: A3A1 DIVIDER.
   - If the test fails, there is a possibility that the A5 synthesizer is faulty. This possibility exists because the A3A1 divider obtains the 40 MHz reference signal from A5. Perform the *1. Check the INT REF Signal* procedure in the *Check A5 Synthesizer Outputs* section. This procedure verifies the 40 MHz reference signal. If the INT REF signal is good, A3A1 is probably faulty. Replace A3A1. If the INT REF signal is bad, replace A5.
2. Press 5, (x1), EXECUTE TEST to run internal test 5: A6 A/D CONVERTER. If the test fails, replace A6.
3. Press 6, (x1), EXECUTE TEST to run internal test 6: A5 REFERENCE OSC. If the test fails, replace A5.
4. Press 7, (x1), EXECUTE TEST to run internal test 7: A5 FRACTIONAL N OSC. If the test fails, replace A5.
5. Press 8, (x1), EXECUTE TEST to run internal test 8: A5 STEP OSC. If the test fails, replace A5.
6. Press 9, (x1), EXECUTE TEST to run internal test 9: A4A1 1st LO OSC. If the test fails, replace A4.
7. Press 1, 3, (x1), EXECUTE TEST to run internal test 13: A3A1 SOURCE OSC. If the test fails, replace A3A1.
8. Press 1, 0, (x1), EXECUTE TEST to run internal test 10: A3A2 2ND LO OSC. If the test fails, replace A3A2.
9. Press 2, 1, (x1), EXECUTE TEST to run external test 21: OUTPUT ATTENUATOR. Then connect the front S and R connectors, and press CONTINUE to start the test. If the test fails, the A7 Output Attenuator is probably faulty. Perform the procedure provided in the *A7 Output Attenuator Control Signals* section to confirm that A7 is faulty.

If all the tests listed above pass and you still believe that the problem is in the source group, verify all the outputs of each assembly in the source group. The procedures to do this are provided in the following sections.

CHECK A5 SYNTHESIZER OUTPUTS

The output signals from the A5 Synthesizer are listed below. The input signal to A5 is the external reference signal from the EXT REF connector. See Figure 7-1. If all the output signals and the HP 4291B operation using the EXT REF input signal are good, A5 is probably good.

- INT REF signal on the rear panel
- FRAC N OSC signal going to A4A1
- STEP OSC signal going to A4A1
- 520 MHz signal going to A3A2
- 40 MHz signal going to A3A1 and A6

Perform the following procedures sequentially to verify all the signals listed above and to verify the HP 4291B operation when the EXT REF signal is used.

In these procedures, the 40 MHz signal is not verified because it is indirectly verified if the INT REF signal is good. The signals are observed using test equipment and the HP 4291B self-test functions. For detailed information about the self-test functions, see the *Service Key Menus*.

1. Check the INT REF Signal

The INT REF signal (10 MHz, +2 dBm typical) on the rear panel is derived from the 40 MHz reference signal through the first and second 1/2 dividers. See the A5 Synthesizer block in Figure 7-1. Perform the following steps to verify the INT REF signal's frequency and level:

a. On the HP 4291B, press the following keys to measure the INT REF frequency by using the bus measurement function:

   (Preset), (Sweep), NUMBER OF POINTS, (2), (x1), (System), SERVICE MENU, SERVICE MODES, BUS MEAS [OFF], FREQ BUS [OFF], (5), (x1), BUS MEAS on OFF (then the label changes to BUS MEAS ON off)

b. Check that the marker reading is 2.5 U ± 0.01 U.

   The frequency bus measures the INT REF frequency (10 MHz) through a 1/4 divider. Therefore, the measured value is 2.5 U (10 MHz divided by 4). The unit "U" in the frequency bus measurement is equivalent to MHz.

   - If the marker reading is good, continue with the next step.
   - If the marker reading is bad, the second 1/2 divider in A5 is probably faulty. Replace A5.

c. Connect the equipment as shown in Figure 7-2.

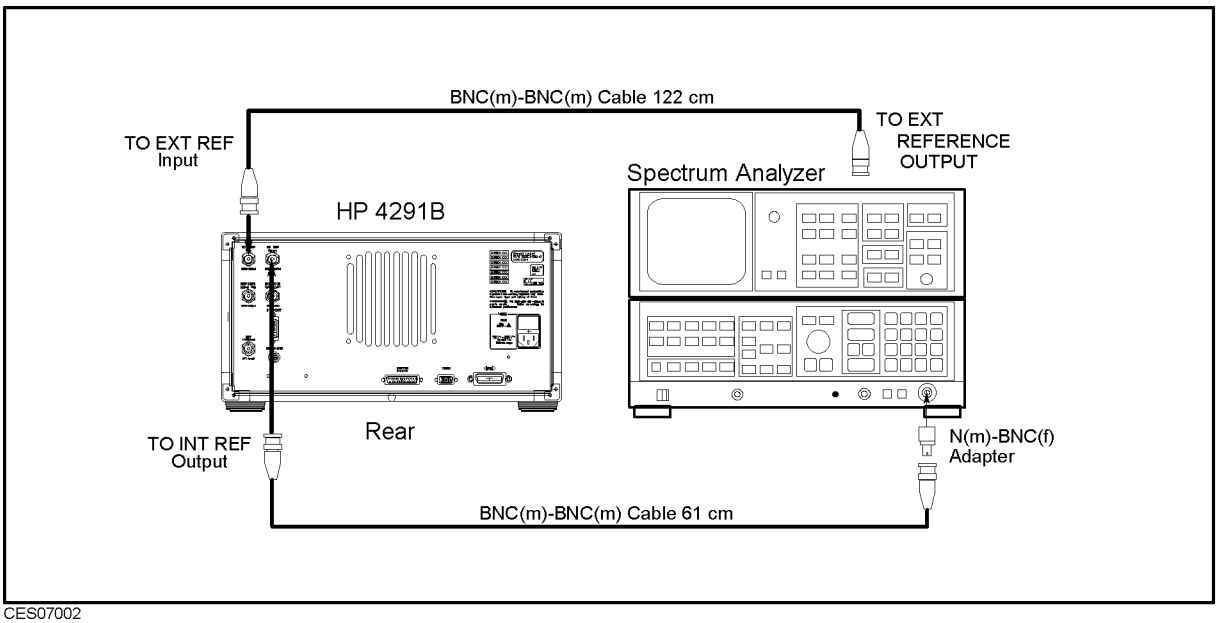


Figure 7-2. INT REF Test Setup

d. Initialize the spectrum analyzer. Then set the controls as follows:

Controls	**Settings**
Center Frequency	10 MHz
Span	15 MHz
Reference Level	10 dBm

e. On the spectrum analyzer, press (PEAK SEARCH) to move the marker to the peak of the INT REF signal.

f. Check that the frequency is approximately 10 MHz and the level is +2 dBm ± 4 dB. The INT REF signal should be as shown in Figure 7-3.

- If the INT REF signal is good, continue with *3. Check the FRAC N OSC Signal.*
- If the INT REF signal is bad, inspect the cable and connections between the INT REF connector and A5J10. See Figure 7-2 for the location of A5J10. If the cable and connections are good, replace A5.

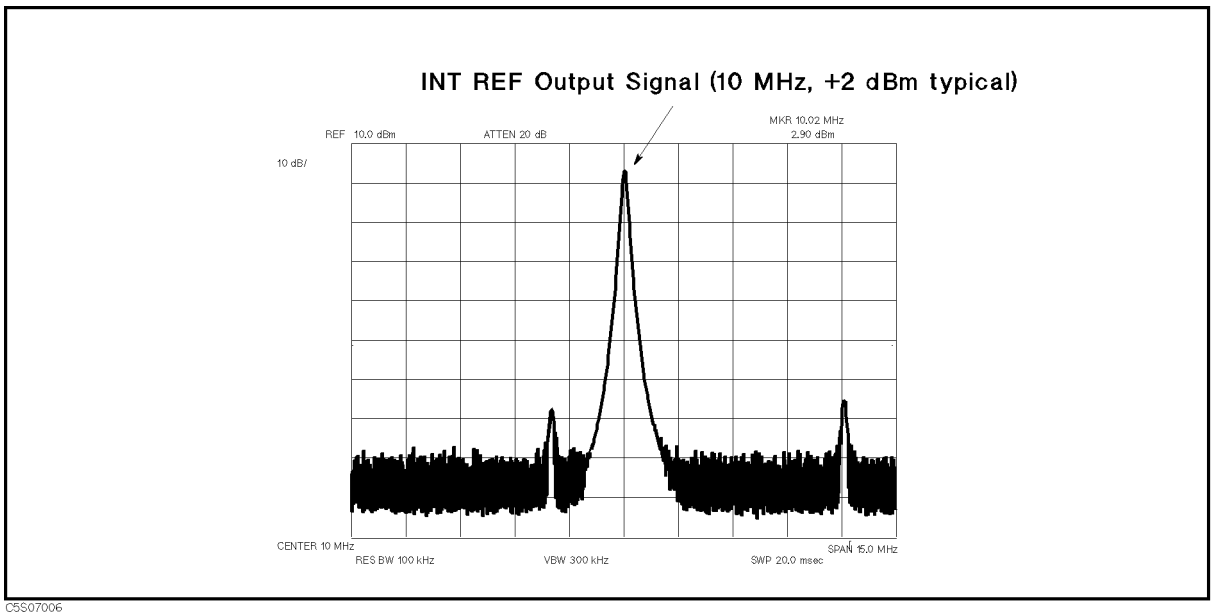


Figure 7-3. Typical INT REF Signal

2. Check the FRAC N OSC Signal

The fractional N oscillator (FRAC N OSC) generates the signal for frequencies from 31.25 MHz to 62.5 MHz. The signal level must be +4.25 dBm ± 5 dB over the frequency range. Perform the following steps to verify the frequency and level of the FRAC N OSC signal:

a. Press the following keys to measure the FRAC N OSC frequency by using the bus measurement function:

(Preset), (System), SERVICE MENU, SERVICE MODES, BUS MEAS [OFF], FREQ BUS [OFF], (4), (x1), BUS MEAS on OFF (then the label changes to BUS MEAS ON off)

b. Wait for the completion of the sweep.

c. Perform the following steps to verify the frequencies of the FRAC N OSC signal:

i. Press (Marker), (1), (M/μ) to move the marker to the start frequency 1 MHz. Then check that the marker reading is 2.0113 U ± 0.01 U.

The frequency bus measures the FRAC N OSC frequency through a 1/16 divider. Therefore, the measured value is 1/16 of the actual frequency. For example, the measured value at the start frequency 1 MHz is 2.0113 U (32.181 MHz divided by 16). The unit "U" in the frequency bus measurement is equivalent to MHz.

ii. Press (Marker), (1), (.), (8), (G/n) to move the marker to the stop frequency 1.8 GHz. Then check that the marker reading is 3.7681 U ± 0.01 U.

iii. Check that the displayed trace is straight (see Figure 7-4).

- If the marker readings and the trace are good, continue with the next step.
- If one (or more) of the marker readings or the trace is bad, the FRAC N OSC is probably faulty. Replace A5.

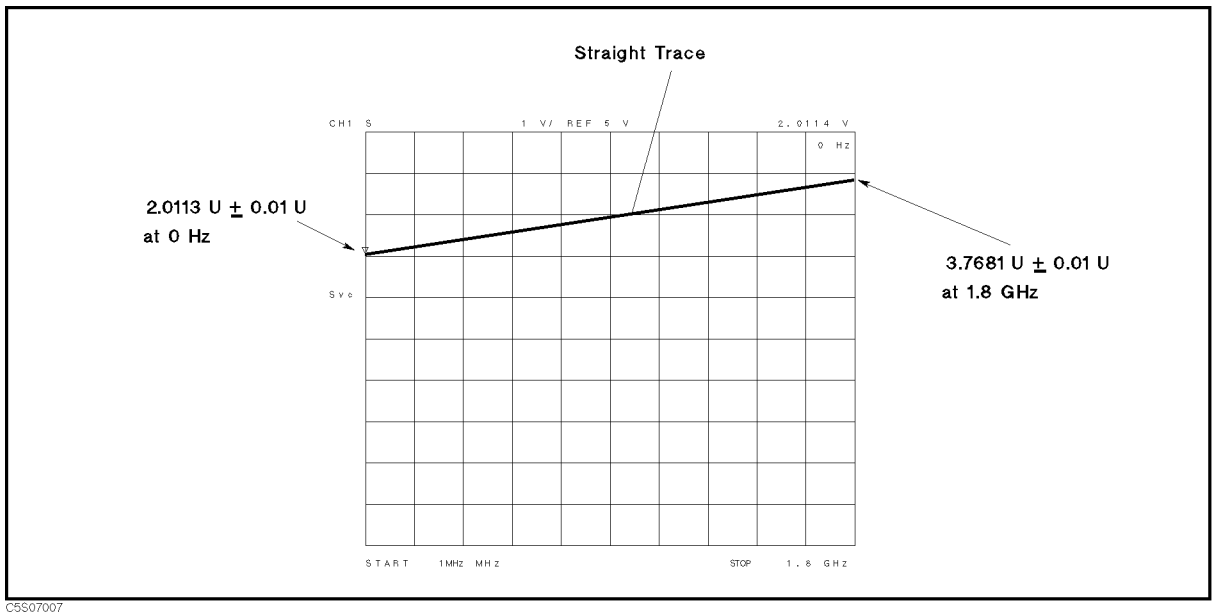


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Figure 7-4. Typical FRAC N OSC Signal in Frequency Bus Measurement

d. Remove the "H" cable from the A5J7 "FN OUT" connector. Then connect the equipment as shown in Figure 7-5.

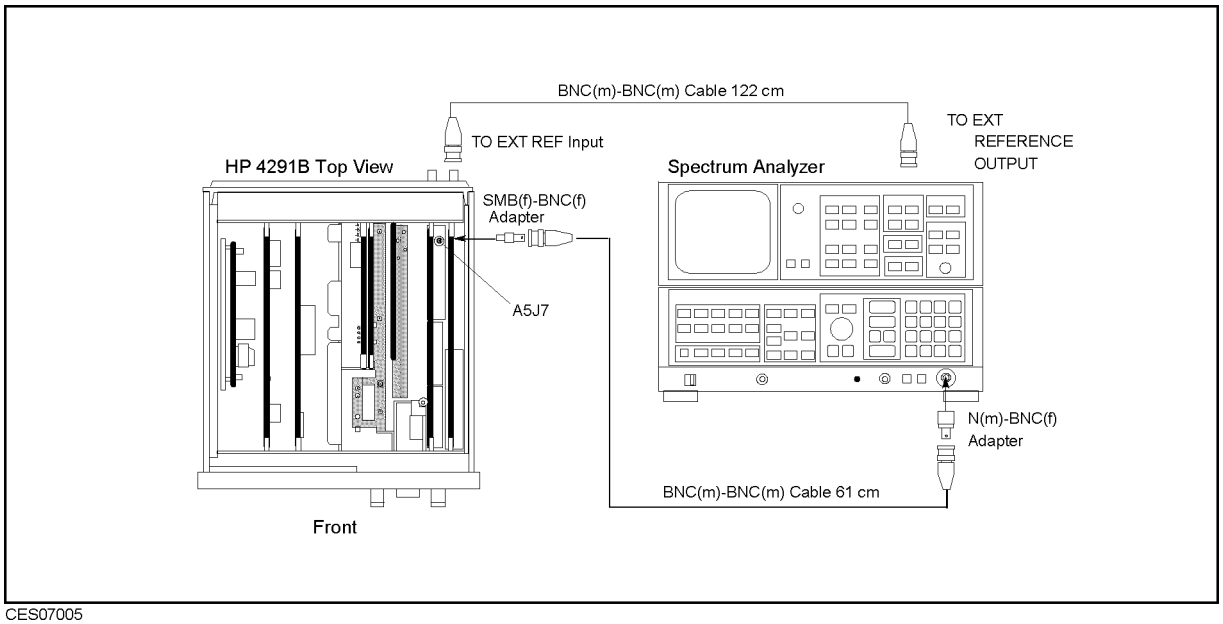

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Figure 7-5. FRAC N OSC Signal Level Test Setup

e. On the HP 4291B, press (Preset), (Sweep), SWEEP TIME, (2), (0), (x1) to set the sweep speed slow enough to check the FRAC N OSC signal with the spectrum analyzer.

f. Press (Trigger), SWEEP HOLD to hold the sweep.

g. Initialize the spectrum analyzer. Then set the controls as follows: (The sweep time must be less than 24 msec.)

Controls	Settings
Start Frequency	30 MHz
Stop Frequency	70 MHz
Reference Level	10 dBm
Max Hold	ON

h. On the HP 4291B, press SINGLE to make a sweep.

i. Wait for the completion of the sweep, and check that the signal level is +4.5 dBm ± 5 dB over the frequency range of 32.18 MHz to 60.29 MHz. The displayed trace should be as shown in Figure 7-6.

- If the signal is good, the FRAC N OSC is working. Continue with the next step.
- If the signal is bad, the FRAC N OSC is faulty. Replace A5.

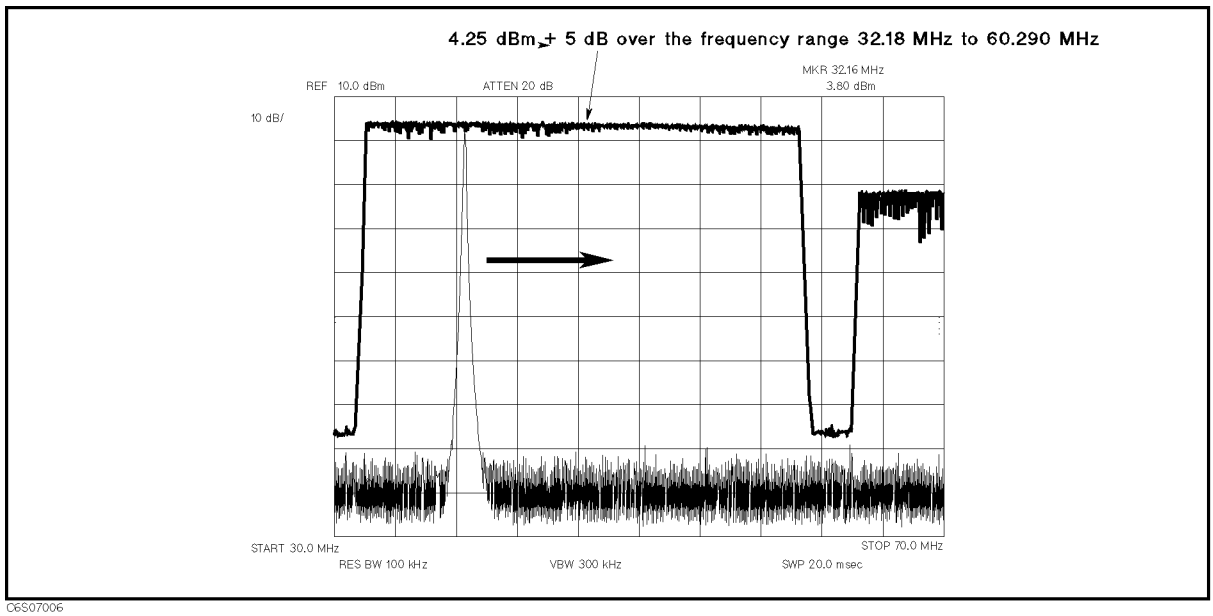

Figure 7-6. FRAC N OSC Typical Signal

j. Reconnect the "H" cable to the A5J7 "FN OUT" connector. Continue with *3. Check the STEP OSC Signal.*

3. Check the STEP OSC Signal

The step oscillator (STEP OSC) generates the signal for frequencies from 470 MHz to 910 MHz with a 20 MHz step. The signal level is typically between −3 dBm and +5 dBm over the frequency range. Perform the following steps to verify the STEP OSC signal:

a. Remove the "L" cable from the A5J2 "STEP PLL OUT" connector. Then connect the equipment as shown in Figure 7-7.

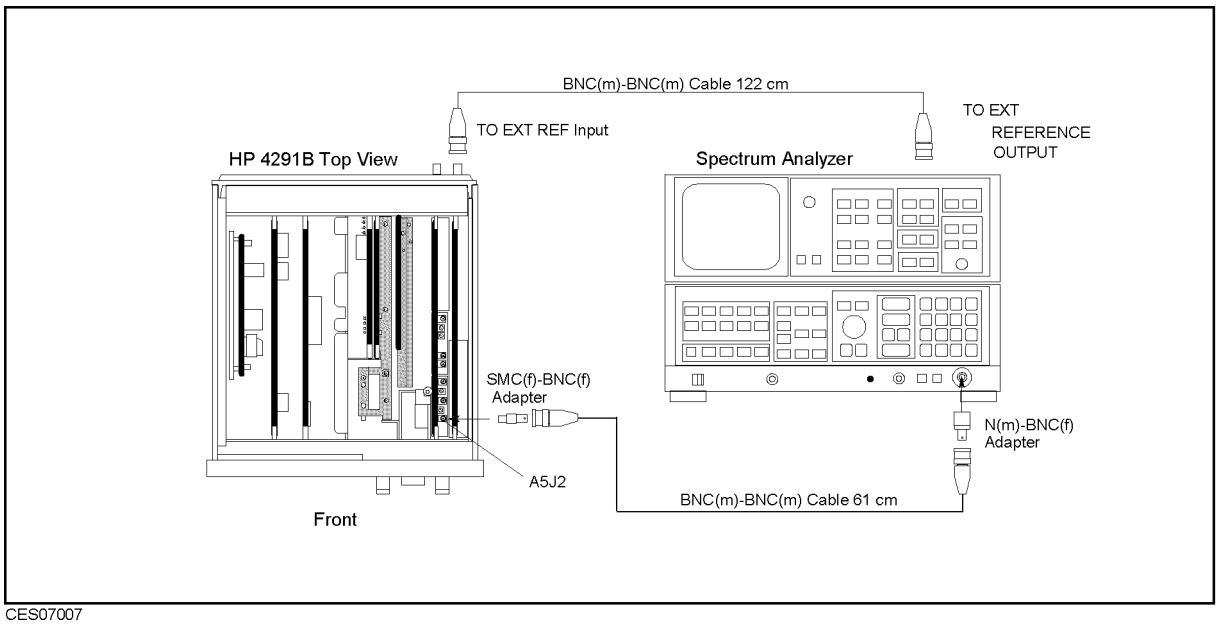

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Figure 7-7. STEP OSC Test Setup

b. On the HP 4291B, press the following keys to measure the STEP OSC frequency by using the bus measurement function:

(Preset), (Sweep), NUMBER of POINTS, (2), (x1), (System), SERVICE MENU, SERVICE MODES, BUS MEAS [OFF], FREQ BUS [OFF], (3), (x1), BUS MEAS on OFF (then the label changes to BUS MEAS ON off)

c. Initialize the spectrum analyzer. Then set the controls as follows:

Controls	**Settings**
Start Frequency	400 MHz
Stop Frequency	1 GHz
Reference Level	10 dBm

d. On the HP 4291B, press (Span), (0), (x1), (Center), (1), (M/μ), to set the center frequency to the first setting of 1 MHz.

e. Perform the following steps to verify the STEP OSC signal at a center frequency of 1 MHz.

i. Check that the HP 4291B marker reading is 1.8359 U $\pm$ 0.01 U.

The frequency bus measures the STEP OSC frequency through a 1/256 divider. Therefore, the measured value is 1/256 of the actual frequency. For example, the measured value at a center frequency of 1 MHz is 1.8359 U (470 MHz divided by 256). The unit "U" in the frequency bus measurement is equivalent to MHz.

ii. On the spectrum analyzer, press (PEAK SEARCH) to move the marker to the peak of the STEP OSC signal, and check that the spectrum analyzer's marker reading is between –3 dBm to +5 dBm.

iii. Check that the trace displayed on the spectrum analyzer is as shown in Figure 7-8.

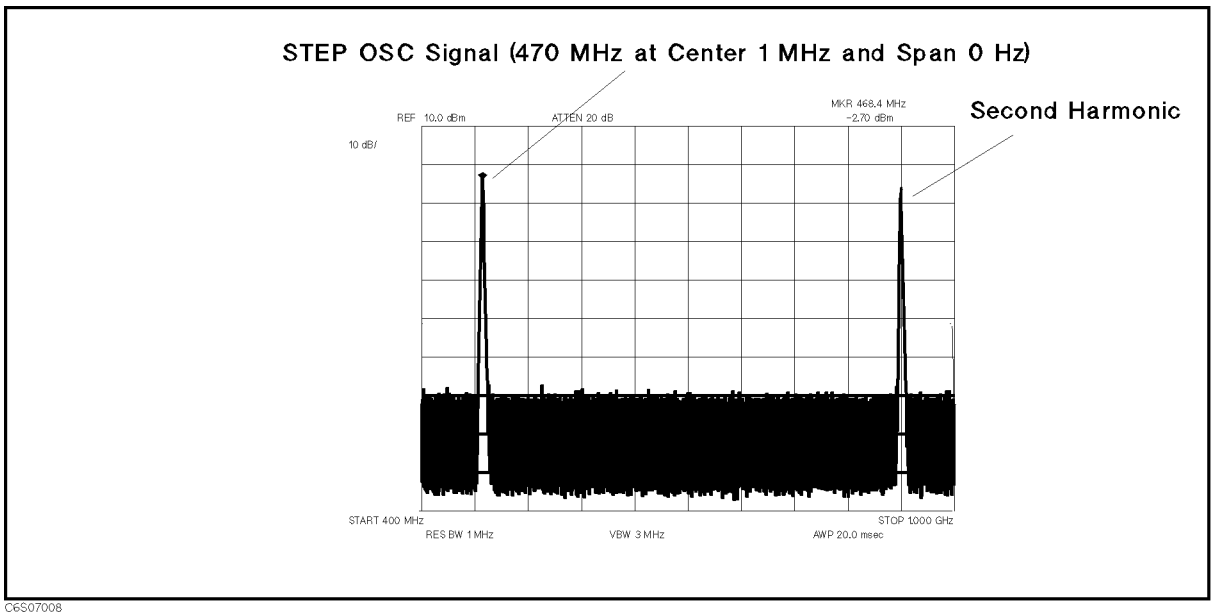

Figure 7-8. Typical STEP OSC Signal at Center 1 MHz

- If the signal is good, continue with the next step.
- If the signal is bad, perform the *Comb Generator Adjustment* and *Step Pretune Correction Constants* procedures (see Chapter 3). If the signal is still bad after the adjustments are performed, the STEP OSC is probably faulty. Replace A5.

f. On the HP 4291B, change the center frequency using numeric keys, and check the STEP OSC signal at the frequencies listed Table 7-1, as the same manner. Table 7-1 lists typical STEP OSC frequencies and their bus measurement limits.

Table 7-1. STEP OSC Frequency

HP 4291B Center Frequency	STEP OSC Frequency	Bus Measurement Limits
1 MHz	470 MHz	1.8359 U ± 0.01 U
80 MHz	490 MHz	1.9140 U ± 0.01 U
160 MHz	510 MHz	1.9921 U ± 0.01 U
240 MHz	530 MHz	2.0703 U ± 0.01 U
320 MHz	550 MHz	2.1484 U ± 0.01 U
400 MHz	570 MHz	2.2265 U ± 0.01 U
480 MHz	590 MHz	2.3046 U ± 0.01 U
560 MHz	610 MHz	2.3828 U ± 0.01 U
640 MHz	630 MHz	2.4609 U ± 0.01 U
720 MHz	650 MHz	2.5390 U ± 0.01 U
800 MHz	670 MHz	2.6171 U ± 0.01 U
880 MHz	690 MHz	2.6953 U ± 0.01 U
960 MHz	710 MHz	2.7734 U ± 0.01 U
1040 MHz	730 MHz	2.8515 U ± 0.01 U
1120 MHz	750 MHz	2.9296 U ± 0.01 U
1200 MHz	770 MHz	3.0078 U ± 0.01 U
1280 MHz	790 MHz	3.0859 U ± 0.01 U
1360 MHz	810 MHz	3.1640 U ± 0.01 U
1440 MHz	830 MHz	3.2421 U ± 0.01 U
1520 MHz	850 MHz	3.3203 U ± 0.01 U
1600 MHz	870 MHz	3.3984 U ± 0.01 U
1680 MHz	890 MHz	3.4765 U ± 0.01 U
1800 MHz	910 MHz	3.5546 U ± 0.01 U

g. Reconnect the "L" cable to the A5J2 "STEP PLL OUT" connector. Continue with *5. Check the 520 MHz Signal.*

4. Check the 520 MHz Signal

The 520 MHz signal (520 MHz, −15 dBm ± 0.2 dB) is derived from the 40 MHz reference signal through the X 13 Multiplier. See the A5 Synthesizer block in Figure 7-1. Therefore, the signal contains 40 MHz harmonics as shown in Figure 7-9. Perform the following steps to verify the 520 MHz signal:

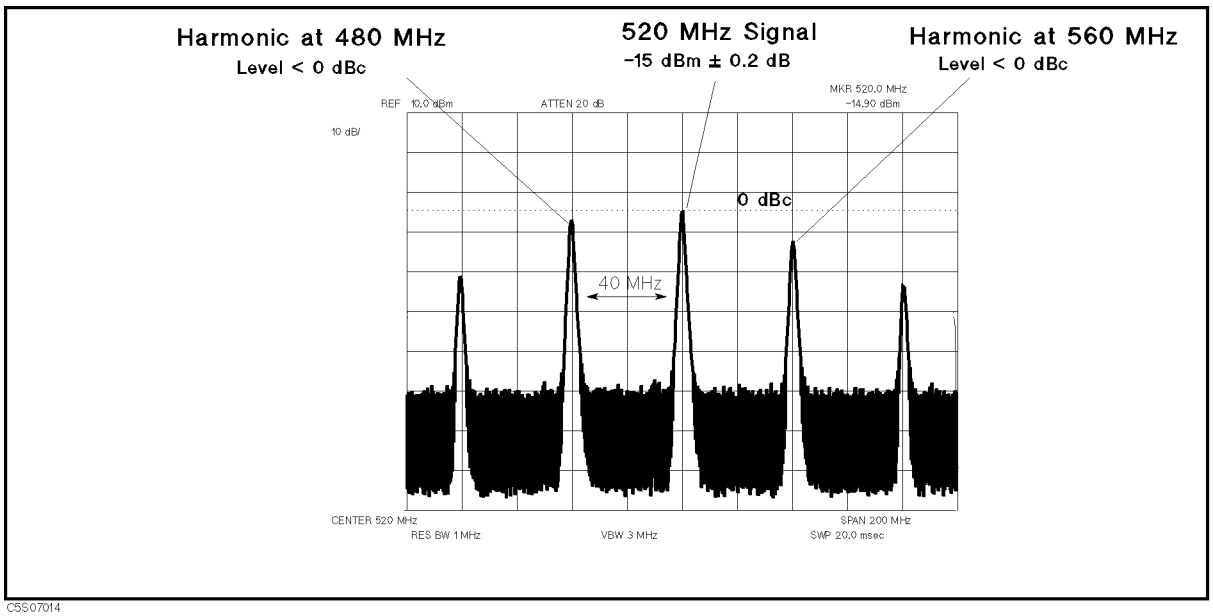

Figure 7-9. Typical 520 MHz Signal

a. Press (Preset) to initialize the HP 4291B.

b. Remove the "J" cable from the A5J3 "520 MHz OUT" connector. After the "PHASE LOCK LOOP UNLOCKED" message appears, connect the equipment as shown in Figure 7-10.

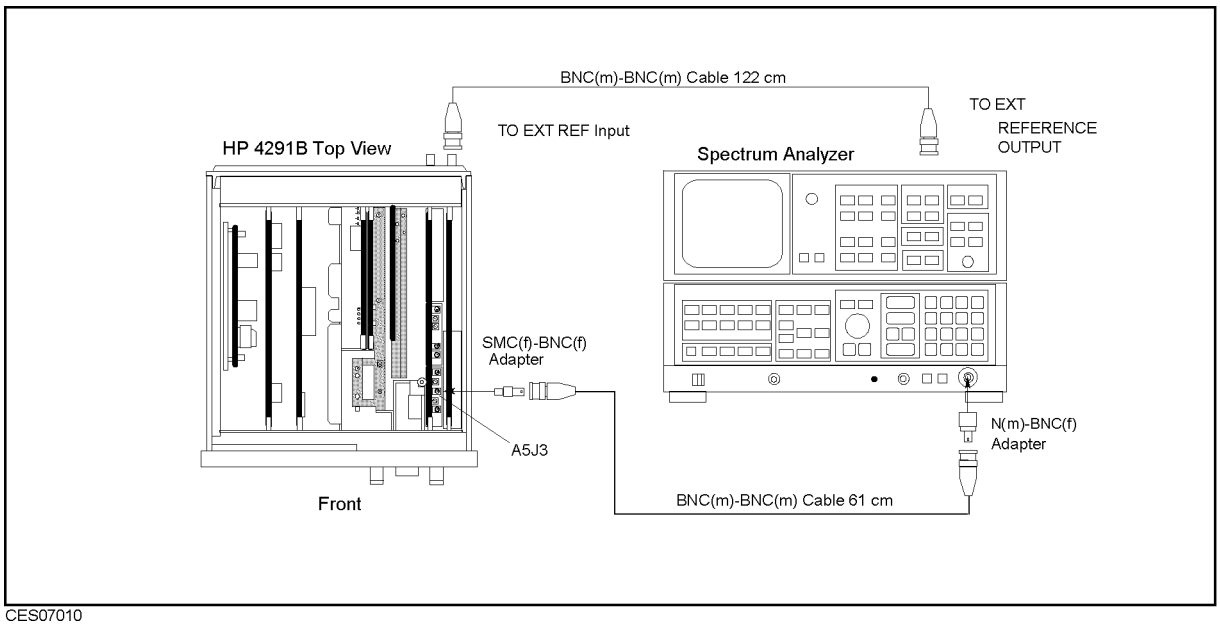

Figure 7-10. 520 MHz Signal Test Setup

c. Initialize the spectrum analyzer. Then set the controls as follows:

Controls	**Settings**
Center Frequency	520 MHz
Span	200 MHz

d. On the spectrum analyzer, press (PEAK SEARCH) to move the marker to the peak of the 520 MHz signal.

e. Check that the frequency is 520 MHz, the level is −15 dBm ± 0.2 dB, and the harmonic levels at 480 MHz and 560 MHz are lower than 0 dBc (lower than the 520 MHz signal level). The trace displayed on the spectrum analyzer should be as shown in Figure 7-14.

- If the signal is good, continue with *5. Check the EXT REF Operation.*
- If the signal level is out of the limits, perform the *520 MHz Level Adjustment* (see Chapter 3).
  - If the adjustment is successfully completed, continue with *5. Check the EXT REF Operation.*
  - If the adjustment fails, the X13 multiplier is faulty. Replace A5.
- If the signal is bad, the X13 multiplier is faulty. Replace A5.

5. Check the EXT REF Operation

When an external reference signal (10 MHz, 0 dBm) is applied to the EXT REF input connector on the rear panel, the message "`ExtRef`" appears on the display. When the external reference signal is removed, the "`ExtRef`" message disappears.

Perform the following steps to verify the operation of the EXT REF input:

a. Connect the equipment as shown in Figure 7-11. Then check that the "`ExtRef`" message appears on the display. If Option 1D5 is installed in the HP 4291B, connect the cable between the EXT REF Input connector and REF OVEN (Opt 1D5) connector.

b. Disconnect the cable from the EXT REF input. Then check that the "`ExtRef`" message disappears.

- If the "`ExtRef`" message appears and disappears correctly, the EXT REF circuit probably working. At this point, the A5 synthesizer is verified.
- If the "`ExtRef`" message does not appear, inspect the cable and connections between the EXT REF input connector and A5J4. See Figure 7-12 for the A5J4 location. If the cable and connections are good, the most probable faulty assembly is A5. Replace A5.

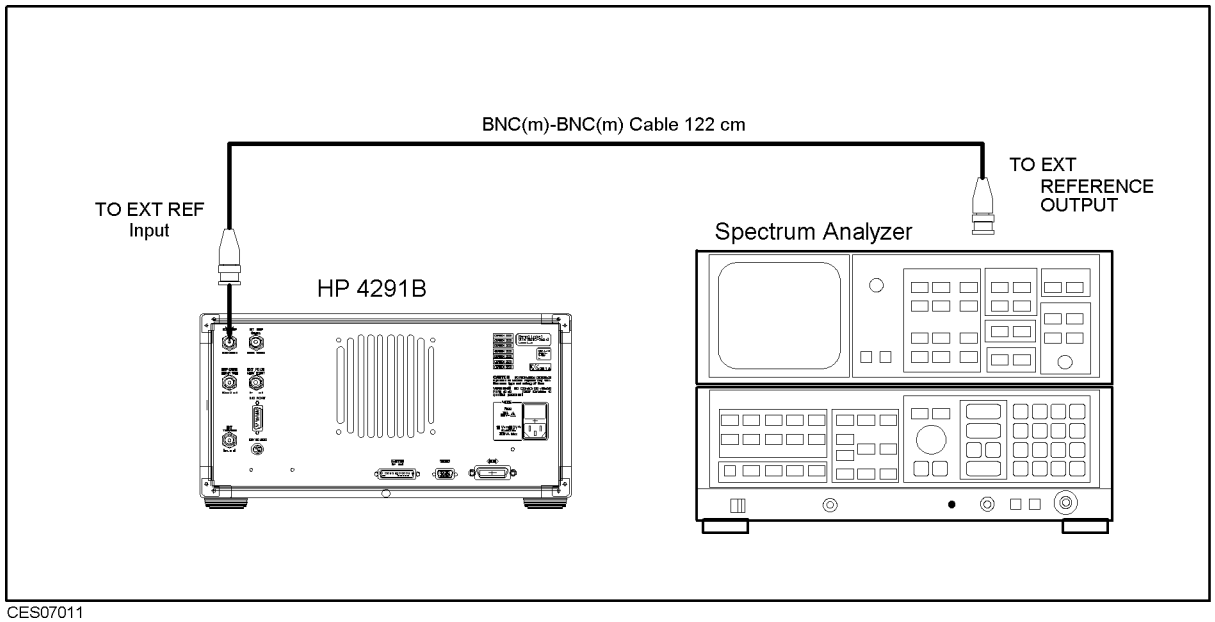

Figure 7-11. EXT REF Test Setup

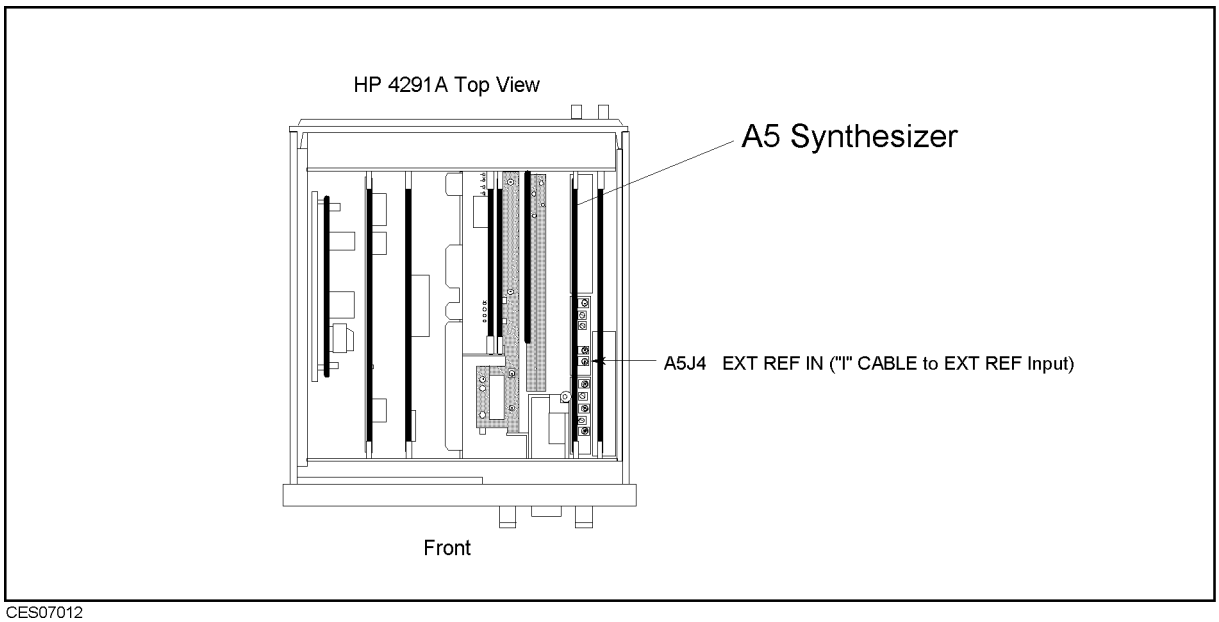

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Figure 7-12. A5J4 Location

CHECK A4A1 1ST LO OUTPUTS

The input signals to A4A1 are the FRAC N OSC signal and the STEP OSC signal (see Figure 7-1). Before performing the procedures in this section, verify the FRAC N OSC signal and STEP OSC signal in accordance with the previous section.

The output signals from A4A1 are two 1st local oscillator signals (2.05858 GHz to 3.85858 GHz). One goes from the A4A1J3 connector to the A3A3 source. The other goes from the A4A1J4 connector to the A4A2 Receiver RF. If the two signals are good, the A4A1 1st LO is verified.

Perform the following procedures sequentially to verify the two A4A1 output signals at A4A1J3 and A4A1J4.

Note If one or both of the signals are bad, the A4A1 1st LO is faulty. Replace the A4 1st LO/Receiver RF (which consists of the A4A1 1st LO and the A4A2 Receiver RF).

In these procedures, the two A4A1 outputs are observed using test equipment and the HP 4291B self-test functions. For detailed information about the HP 4291B self-test functions, see the *Service Key Menus*. Also, the signals are verified in two A4A1 operation modes, single-loop mode and triple-loop mode. For a description of these operation modes, see Chapter 11.

1. Check the 1st LO OSC Signal at A4A1J3

The 1st local oscillator signal at A4A1J3 is a swept 2.05958 GHz to 3.85858 GHz signal with the power level between −5 dBm to +5 dBm over the frequency range. Perform the following steps to verify the 1st local oscillator signal at A4A1J3:

a. Remove the "C" semi-rigid cable from A4A1J3, and connect the equipment as shown in Figure 7-13. In this procedure, connect the spectrum analyzer input to A4A1J3.

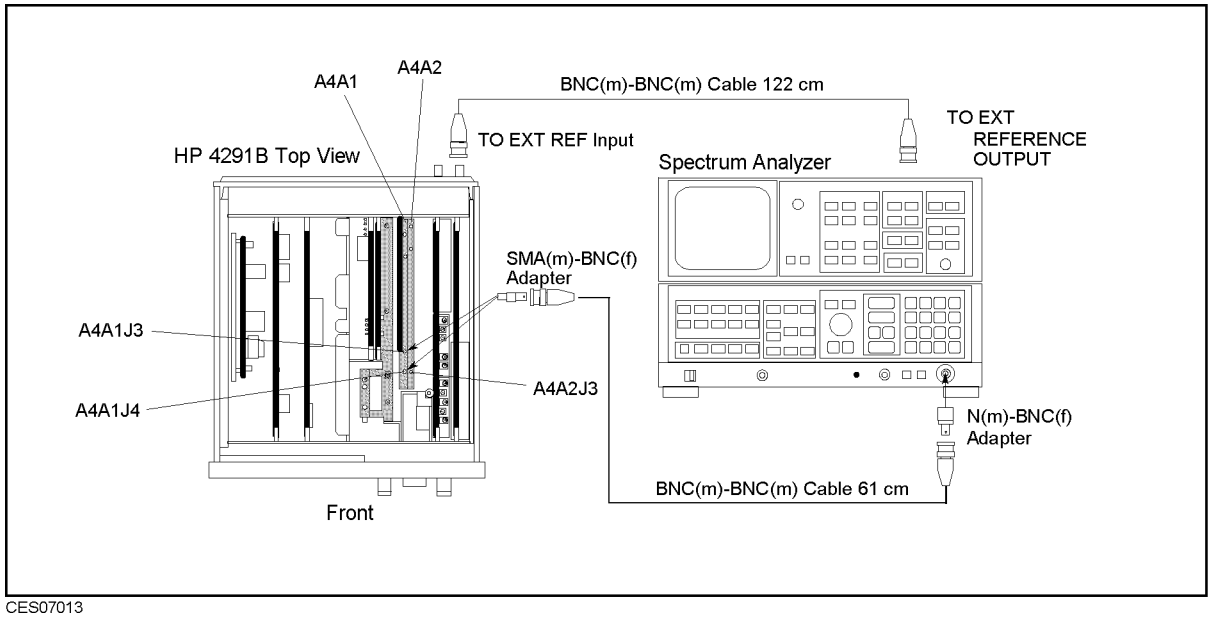


Figure 7-13. 1st LO OSC Signal Test Setup

b. Press (Preset), (Sweep), SWEEP TIME, (2), (0), (x1), (Trigger), SWEEP: HOLD.

During this procedure, the start and stop frequencies are set to 1 MHz and 1.8 GHz, respectively. These start and stop settings set the 1st LO OSC to the single-loop mode and sweep the frequency from 2.05958 GHz (at the start frequency 1 MHz) to 3.85858 GHz (at the stop frequency 1.8 GHz).

c. Initialize the spectrum analyzer. Then set the controls as follows: (The sweep time must be less than 24 msec.)

Controls	**Settings**
Start Frequency	2 GHz
Stop Frequency	4 GHz
Reference Level	10 dBm
Max Hold	ON

d. On the HP 4291B, press SINGLE to make a sweep.

e. Wait for the completion of the sweep, and check that the signal level is −5 dBm to +5 dBm over the frequency range of 2.059 GHz to 3.858 GHz. The displayed trace should be as shown in Figure 7-14.

The measured level is lower than the actual level due to the BNC(m)-BNC(m) cable's insertion loss at high frequencies. If the measured level is lower than the limit, measure the cable's loss and compensate the signal level by the cable's loss.

- If the signal level and the trace are good, continue with the next step.
- If the signal level or the trace is bad, the A4A1 1st LO is faulty. Replace A4.

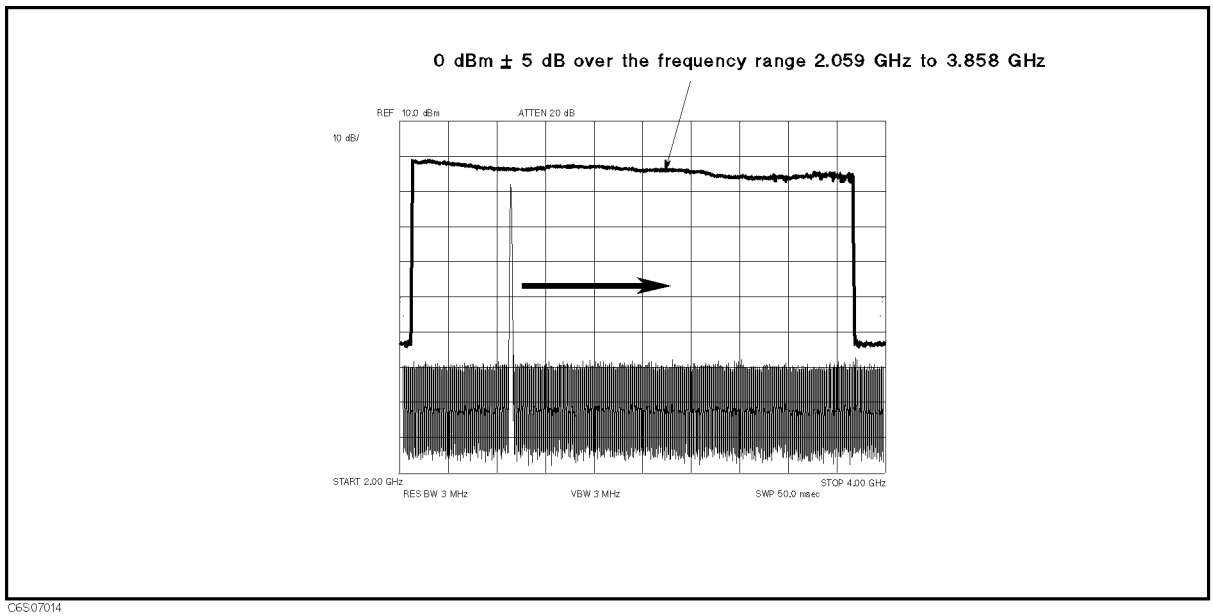


Figure 7-14. Typical 1st LO OSC Signal (Single Mode) at A4A1J3

f. On the HP 4291B, press (Center), (9), (0), (0), (M/μ), (Span), (4), (5), (M/μ).

During this procedure, the start and stop frequencies are set to 877.5 MHz and 922.5 MHz, respectively. These start and stop settings set the 1st LO OSC to the triple-loop mode and sweep the 1st LO OSC frequency from 2.93608 GHz (at the start frequency 877.5 MHz) to 2.98108 GHz (at the stop frequency 922.5 GHz).

g. Initialize the spectrum analyzer. Then set the controls as follows: (The sweep time must be less than 24 msec.)

Controls	Settings
Start Frequency	2.9 GHz
Stop Frequency	3 GHz
Reference Level	10 dBm
Max Hold	ON

h. On the HP 4291B, press SINGLE to make a sweep.

i. Wait for the completion of the sweep, and check that the signal level is −5 dBm to +5 dBm over the frequency range of 2.936 GHz to 2.981 GHz. The displayed trace should be as shown in Figure 7-15.

The measured level is lower than the actual level due to the BNC(m)-BNC(m) cable's insertion loss in the high frequency range. If the measured level is lower than the limit, measure the cable's loss and compensate the signal level by the cable's loss.

- If the signal level and the trace are good, continue with the next step.
- If the signal level or the trace is bad, the A4A1 1st LO is faulty. Replace A4.

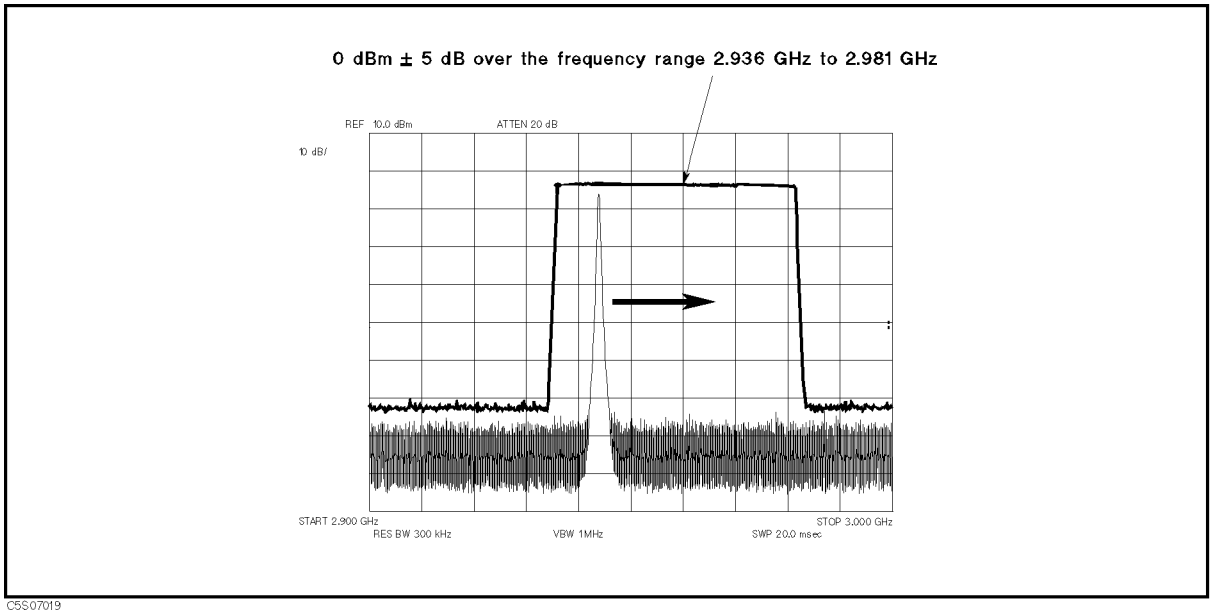


Figure 7-15. Typical 1st LO OSC Signal (Triple Mode) at A4A1J3

j. Reconnect the "C" semi-rigid cable to A4A1J3. Then continue with *2. Check the 1st LO OSC Signal at A4A1J4.*

2. Check the 1st LO OSC Signal at A4A1J4

The 1st local oscillator signal at A4A1J4 is a swept 2.05958 GHz to 3.85858 GHz signal with the power level > +16 dBm over the frequency range. Perform the following steps to verify the 1st local signal at A4A1J4:

a. Remove the "F" semi-rigid cable from A4A1J4 and A4A2J3, and connect the equipment as shown in Figure 7-13. In this procedure, connect the spectrum analyzer input to A4A1J4.

b. On the HP 4291B, press (Preset), (Sweep), SWEEP TIME, (2), (0), (x1), (Trigger), SWEEP: HOLD.

During this procedure, the start and stop frequencies are set to 1 MHz and 1.8 GHz, respectively.

c. Initialize the spectrum analyzer. Then set the controls as follows:

Controls	Settings
Start Frequency	2 GHz
Stop Frequency	4 GHz
Reference Level	20 dBm
Max Hold	ON

d. On the HP 4291B, press SINGLE to make a sweep.

e. Wait for the completion of the sweep, and check that the signal level is higher than +16 dBm over the frequency range of 2.059 GHz to 3.858 GHz. The displayed trace should be as shown in Figure 7-16.

The measured level is lower than the actual level due to the BNC(m)-BNC(m) cable's insertion loss in the high frequency range. If the measured level is lower than the limit, measure the cable's loss and compensate the signal level by the cable's loss.

- If the signal level and the trace are good, continue with the next step.
- If the signal level or the trace is bad, the A4A1 1st LO is faulty. Replace A4.

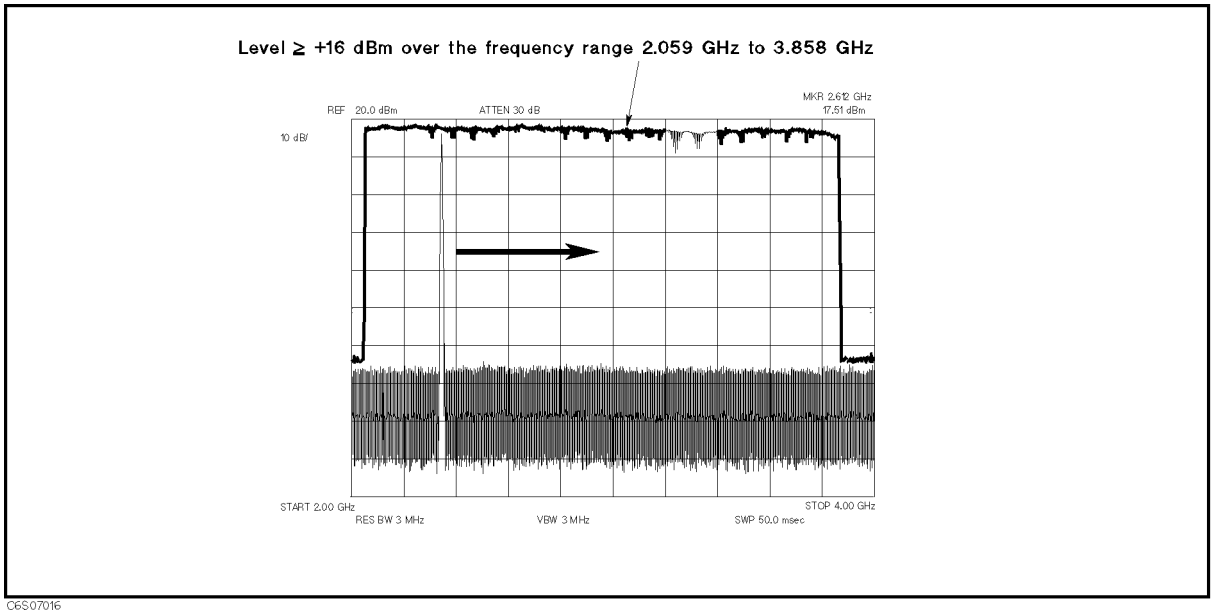


Figure 7-16. 1st LO OSC Typical Signal (Single Mode) at A4J4

f. Reconnect the “F” semi-rigid cable to A4A1J4 and A4A2J3. At here, the A4A1 1st LO is verified.

CHECK AN A3A1 SOURCE VERNIER OUTPUT

The input signal to the A3A1 Source Vernier is the 40 MHz reference signal coming from A5 (see Figure 7-1). Before performing the procedures in this section, verify the INT REF signal in accordance with the *Check A5 Synthesizer Outputs* section. This ensures that the 40 MHz reference signal is good.

The three output signals from A3A1 are the 21.42 MHz signal with the level controlled by the level vernier, the 8 MHz reference signal, and the 40 kHz reference signal.

Perform the following procedures sequentially to verify the 21.42 MHz signal. If the signal is bad, replace A3A1.

In this procedure, only the 21.42 MHz signal is verified. This is because the 8 MHz and 40 kHz reference signals are verified by running internal test 11 in the *Start Here*.

The 21.42 MHz signal is observed using test equipment and its level is controlled by the HP 4291B self-test functions. For detailed information about the HP 4291B self-test functions, see the *Service Key Menus*.

1. Check the 21.42 MHz Signal

Perform the following steps to verify the 21.42 MHz signal:

a. Remove the "D" cable from A3A2J22, and connect the equipment as shown in Figure 7-17.

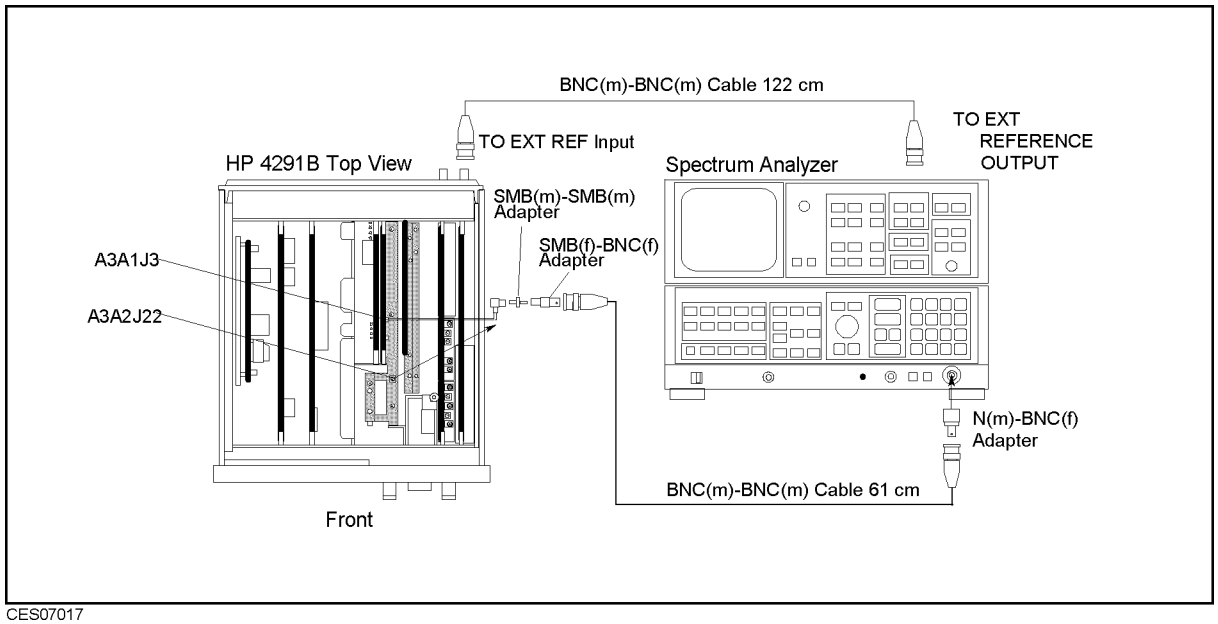


Figure 7-17. 21.42 MHz Signal Test Setup

b. Press (Preset) to initialize the HP 4291B.

c. Initialize the spectrum analyzer. Then set the controls as follows:

Controls	Settings
Center Frequency	21.42 MHz
Span	1 MHz
Reference Level	0 dBm

d. On the HP 4291B, press the following keys to set the OSC DAC value to 13,000.

(System), SERVICE MENU, SERVICE MODES, OSC, OSC AUTO man (then the label changes to OSC auto MAN), OSC DAC AUTO man (then the label changes to OSC DAC auto MAN), OSC DAC VALUE, (1), (3), (0), (0), (0), (x1)

e. On the spectrum analyzer, press (PEAK SEARC) to move the marker to the peak of the 21.42 MHz signal.

f. Check that the frequency is 21.42 MHz and the level is higher than – 18 dBm. The displayed trace should be as shown in Figure 7-18.

- If the signal is good, A3A1 is verified.
- If the signal is bad, replace A3A1.

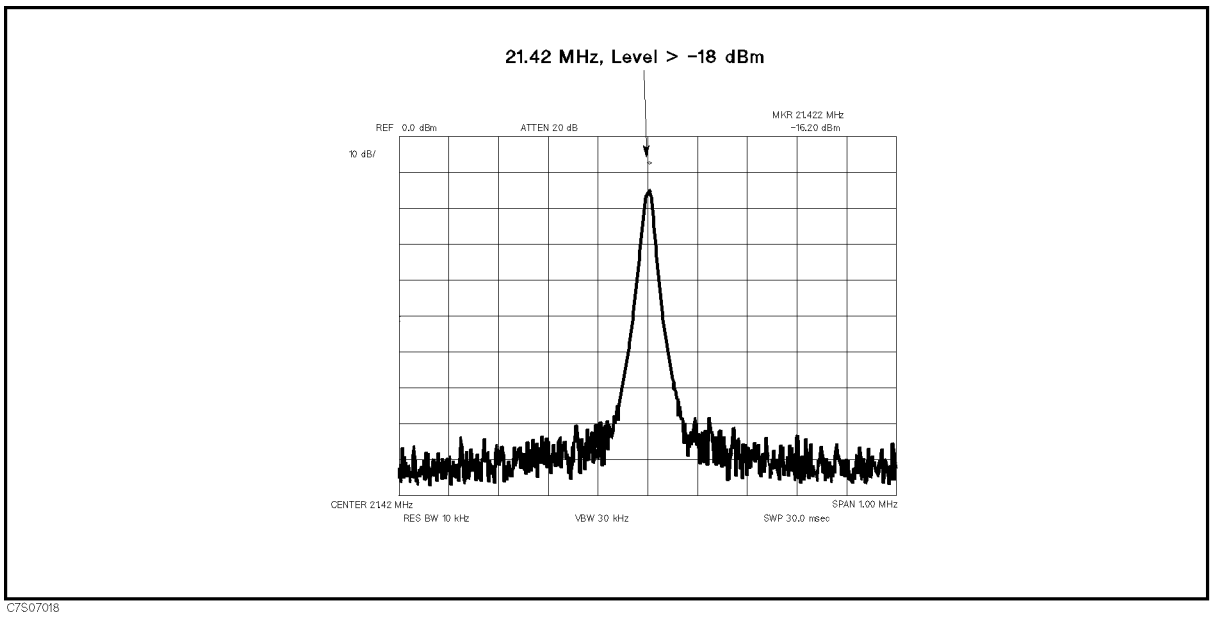


Figure 7-18. Typical 21.42 MHz Signal

CHECK A3A2 2ND LO OUTPUTS

The two input signals to A3A2 are the 520 MHz signal coming from A5 and the 21.42 MHz signal coming from A3A1. See Figure 7-1. Before performing the procedures in this section, verify the 520 MHz signal in accordance with the *Check A5 Synthesizer Outputs* section and verify the 21.42 MHz signal in accordance with the *Check an A3A1 Source Vernier Output* section.

The two output signals from A3A2 are the 2.08 GHz 2nd local oscillator signal going to the A4A2 Receiver IF and the 2.05858 GHz signal going to the A3A3 source. Perform the following procedures sequentially to verify these signals. If one of the signals is bad, replace A3A2.

In this procedure, the 2.05858 GHz signal level is controlled by the HP 4291B self-test functions. For detailed information about the HP 4291B self-test functions, see the *Service Key Menus*.

1. Check the 2nd Local Oscillator Signal

The 2nd local oscillator signal is the 2.08 GHz CW signal a with signal level > +7 dBm (typical). Perform the following steps to verify the frequency and level of the 2nd local oscillator signal:

a. Remove the "I" semi-rigid cable from A3A2J19 and remove the "D" cable from A3A1J3. See Figure 7-19 for the locations of A3A2J19 and A3A1J3. Then connect the equipment as shown in Figure 7-19.

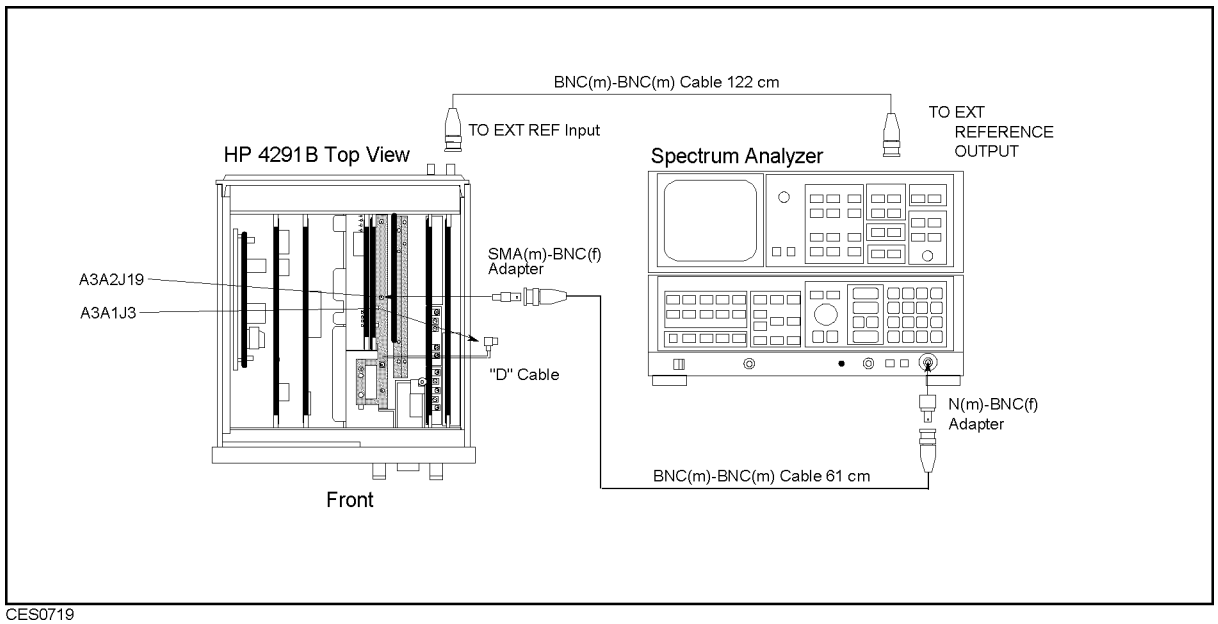


Figure 7-19. 2nd LO OSC Test Setup

b. Initialize the spectrum analyzer. Then set the controls as follows:

Controls	Settings
Center Frequency	2.08 GHz
Span	1 MHz
Reference Level	20 dBm

c. On the spectrum analyzer, press (PEAK SEARCH) to move the marker to the peak of the 2nd Local.

d. Check that the frequency is 2.08 GHz and the level is higher than +7 dBm. The 2nd local oscillator signal should be as shown in Figure 7-20.

The measured level is lower than the actual level due to the BNC(m)-BNC(m) cable's insertion loss at high frequency. If the measured level is lower than the limit, measure the cable's loss and compensate the signal level by the cable's loss.

- If the signal is good, continue with the next step.
- If it is bad, perform the *Second Local PLL Lock Adjustment* (see Chapter 3). If the problem persists after the adjustment, the A3A2 2nd LO OSC is faulty. Replace A3A2.

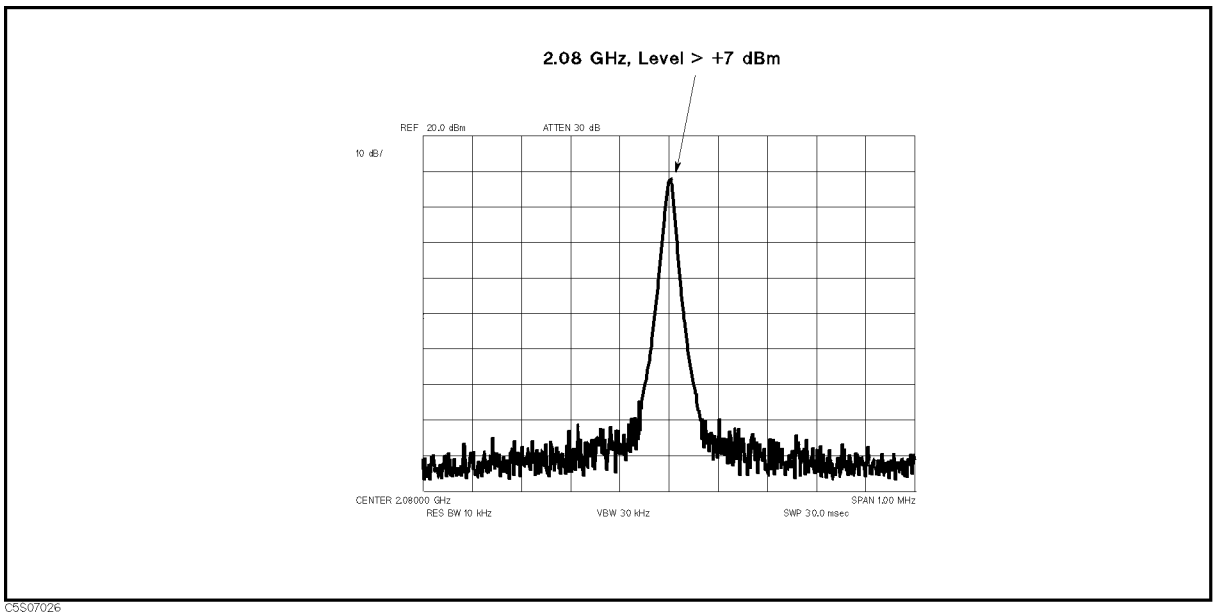


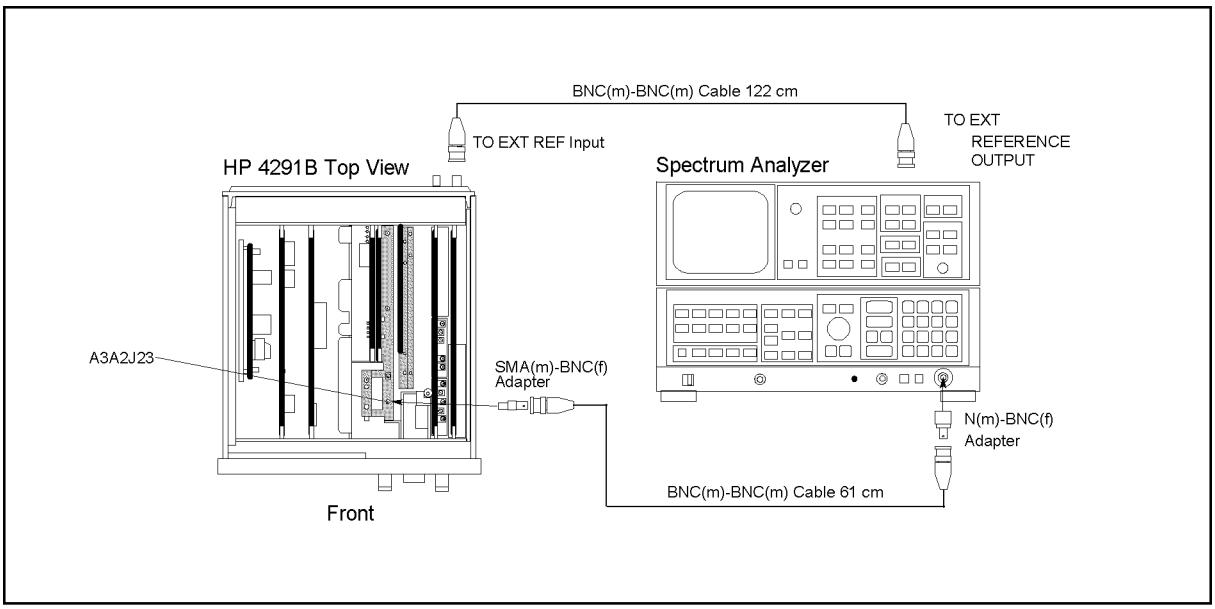
Figure 7-20. Typical 2nd Local Oscillator Signal

e. Reconnect the "I" semi-rigid cable to A3A2J19 and reconnect the "D" cable to A3A1J3. Then continue with *2. Check the 2.05858 GHz Signal.*

2. Check the 2.05858 GHz Signal

The 2.05858 GHz signal level is controlled by the ALC loop. See the A3A2 2nd LO block in Figure 7-1. Perform the following steps to verify the frequency and level of the 2.05858 GHz signal:

a. Remove the "E" cable from A3A2J23. See Figure 7-21 for the location of A3A2J23. Then connect the equipment as shown in Figure 7-21.



CES07021

Figure 7-21. 2.05858 GHz Signal Test Setup

b. Press (Preset) to initialize the HP 4291B.

c. Initialize the spectrum analyzer. Then set the controls as follows:

Controls	**Settings**
Center Frequency	2.05858 GHz
Span	1 MHz
Reference Level	0 dBm

d. On the HP 4291B, press the following keys to set the OSC level control DAC value to 13,000.

(System), SERVICE MENU, SERVICE MODES, OSC, OSC AUTO man (then the label changes to OSC auto MAN), OSC DAC AUTO man (then the label changes to OSC DAC auto MAN), OSC DAC VALUE, (1), (3), (0), (0), (0), (x1)

e. On the spectrum analyzer, press (PEAK SEARCH) to move the marker to the peak of the ALC output signal.

f. Check that the frequency is 2.05858 GHz and the level is higher than −13 dBm. The displayed trace should be as shown in Figure 7-22.

- If the signal is good, continue with the next step.
- If the signal is bad, the Source First Mixer is faulty. Replace A3A2.

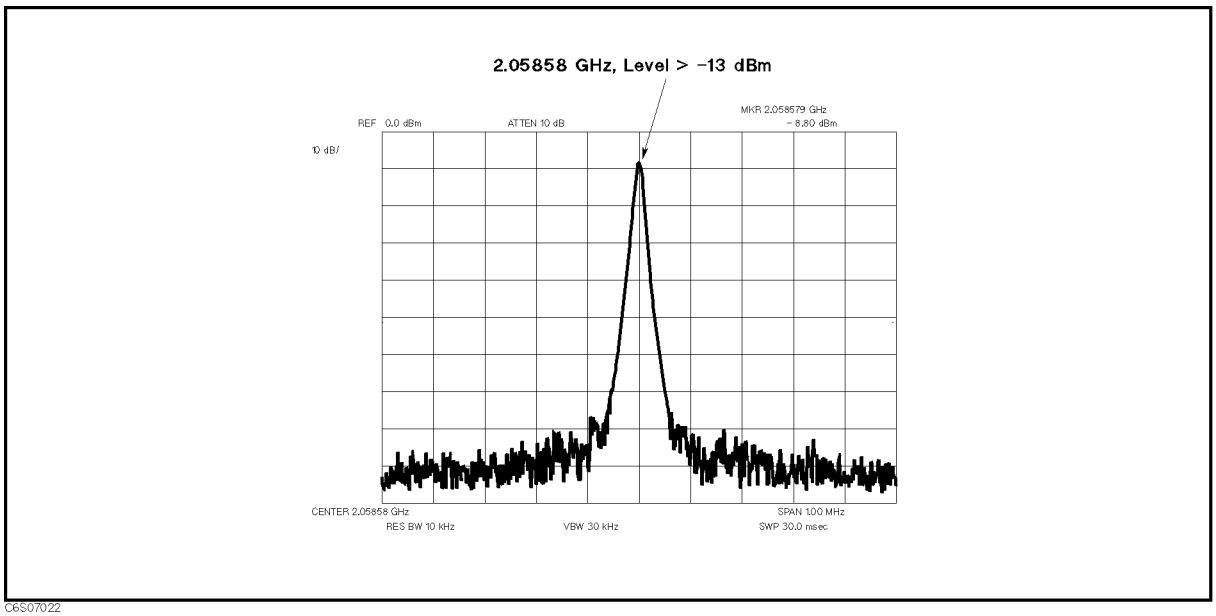


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Figure 7-22. Typical 2.05858 GHz Signal

g. Reconnect the “E” semi-rigid cable to A3A2J23. At this point, the A3A2 2nd LO is verified.

CHECK A3A3 SOURCE OUTPUT

The two input signals to A3A3 are the 1st local oscillator signal coming from A4A1 and the 2.05858 GHz signal coming from A3A2. See Figure 7-1. Before performing the procedures in this section, verify the 1st local oscillator signal at A4A1J3 in accordance with the *Check A4A1 1st LO Outputs* section and verify the 2.05858 GHz signal in accordance with the *Check A1A2 2nd LO Outputs*.

The two output signals from A3A3 are the RF signal (100 kHz to 1.8 GHz, −10 dBm to +20 dBm) going to the A7 output attenuator and the level detector's signal going to the A3A1 Source Vernier. Only the RF signal is checked in the following procedure, because the level detector's signal were already verified in internal test 15: SOURCE LEVEL.

Perform the following procedure to verify the RF signal. If the signal is bad, replace A3A3.

1. Check the A3A3 RF Signal

The A3A3 source generates the RF signal (1 MHz to 1.8 GHz). Perform the following steps to verify the frequency and level of the RF signal:

a. Connect the power sensor to the power meter, and calibrate the power meter for the power sensor.

b. Connect the equipment as shown in Figure 7-23.

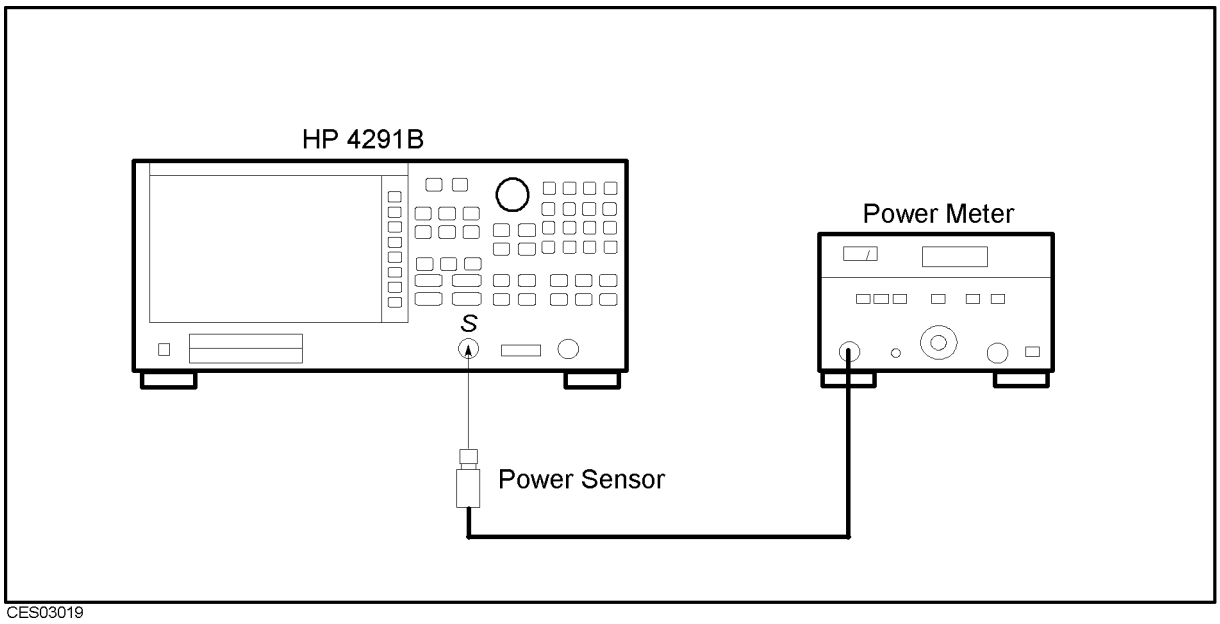

Figure 7-23. A3A3 RF Signal Test Setup

c. Press the following keys to set the first setting of the RF signal test. (Preset), (System), `Service Menu`, `Service Modes`, `OSC`, `OSC AUTO man` (then the label changes to `OSC auto MAN`), `OUTPUT ATT [AUTO]`, `0 dB`, (then the label changes to `OUTPUT ATT [0 dB]`), `OSC DAC AUTO man` (then the label changes to `OSC DAC auto MAN`), `OSC DAC VALUE`, (1), (0), (0), (0), (x1), (Span), (0), (x1), (Center), (1), (M/μ)

d. Check that the power meter reading is 0 ±6 dBm.

- If the signal level is good, continue with the next step.
- If the signal level is bad, A3A3 is the most probable faulty assembly. Replace A3A3.

e. Perform the above check for all the settings listed in Table 7-2.

Table 7-2. A3A3 RF Signal Test Settings

Frequency	Output ATT	OSC DAC	Test Limit
1 MHz	0 dB	1000	0 dBm ±6 dB
1 GHz	0 dB	3222	6 dBm ±6 dB
1.8 GHz	0 dB	5000	4 dBm ±6 dB
1.8 GHz	10 dB	32000	> 2.5 dBm

- If all the signal levels are good, A3A3 is verified.
- If any signal level is bad, A3A3 is the most probable faulty assembly. Replace A3A3.

CHECK A7 OUTPUT ATTENUATOR CONTROL SIGNALS

Use this procedure when the A7 Output Attenuator is the most suspicious assembly (for example, if external test 20 fails).

A7 is controlled by the three signals at A7J1, A7J2, and A7J3 that come from the A2 post-regulator.

Perform the following procedure to verify the A7 control signals. If the signals are good, replace A7. If the signals are bad, replace A2.

In this procedure, the control signal is set using the HP 4291B self-test functions. For detailed information about the HP 4291B self-test functions, see the *Service Key Menus*.

1. Check A7 Control Signals

The A7 Output Attenuator is controlled by the three lines at A7J1, A7J2, and A7J3 as shown in Figure 7-23. Perform the following steps to verify the A7 control signals:

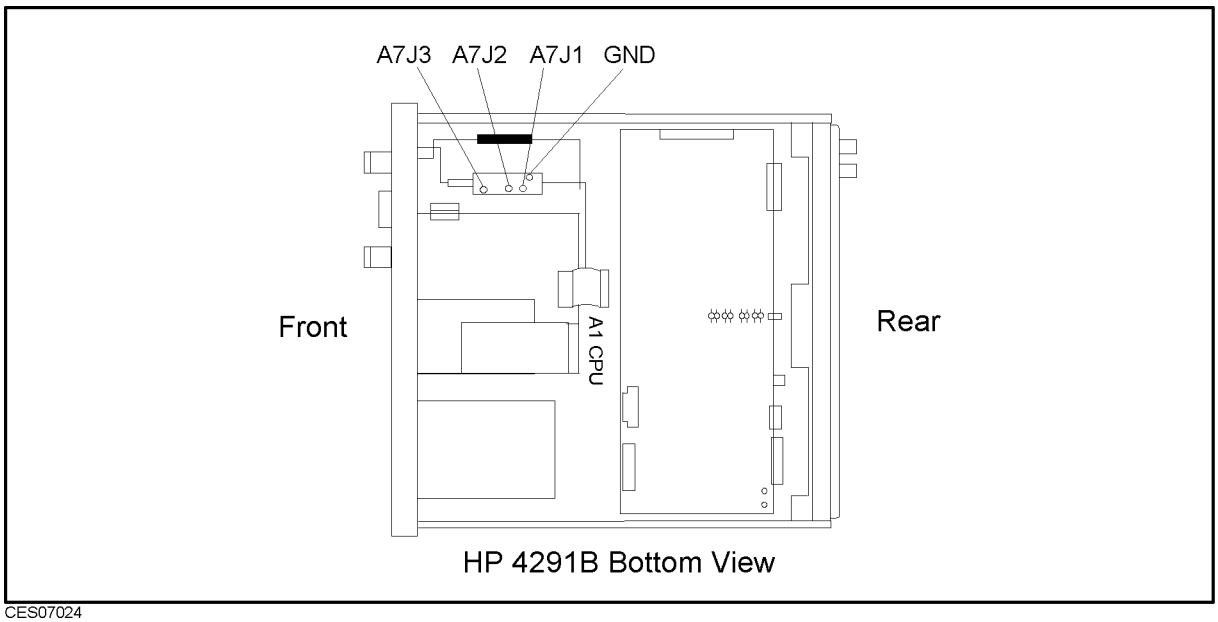

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Figure 7-24. A7 Output Attenuator Control Signals

a. Press the following keys to set the HP 4291B OSC level to manual mode.

   (Preset), (Source), (0), (x1), (System), Service Menu, Service Modes, OSC, OSC AUTO man (then the label changes to OSC auto MAN)

b. On the HP 4291B, press OUTPUT ATT [AUTO], 0 dB to set A7 to the first test setting of 0 dB in Table 7-3.

c. Measure the voltage at A7J1, A7J2, and A7J3 using a voltmeter. Then check the measured values are within limits. The typical voltages are listed in Table 7-3.

   - If the control voltages are good, continue with the next step.
   - If the control voltages are bad, inspect the cable between A7 and A20J20. If the cable is good, the attenuator control circuit in the A2 post-regulator is probably faulty. Replace A2.

Table 7-3. A7 Attenuation Test Settings

A7 Attenuation	A7J1 Voltage	A7J2 Voltage	A7J3 Voltage
0 dB	High[1]	Low[2]	Low
−10 dB	Low	Low	Low
−20 dB	High	High	Low
−30 dB	Low	High	Low
−40 dB	Low	Low	High
−50 dB	High	High	High
−60 dB	Low	High	High

1 Is within +8.4 V to +16 V (+12 V typical).

2 Is 0 V typical.

d. Repeat steps b and c to check A7 in accordance with Table 7-3.

At this point, the A7 attenuator control signals are verified.

CHECK A22 DC BIAS 1/2 OUTPUT

Use this procedure for a DC bias out failure to isolate the trouble between A22 and A23. The HP 4291B DC bias circuit consists of A22 and A23 as shown in Figure 7-1. Therefore, if A22 is operating correctly A23 should be faulty.

Perform the following procedures to verify the A22 output. If the output is bad, replace A22. Otherwise, replace A23.

In this procedure, the control signal is set using the HP 4291B service functions. For detailed information about the service functions, see the *Service Key Menus*.

1. Check A22 Output Voltages

A22 generates the DC bias voltage control signal and current control signal. The voltage control signal voltage is about 1/10 of the DC bias voltage output. The current control signal voltage is about 500/9 [V/A] of the DC bias current output. Perform the following steps to verify A22 output voltages:

a. Turn the HP 4291B off, and remove the flat cable designated ① in Figure 7-25.

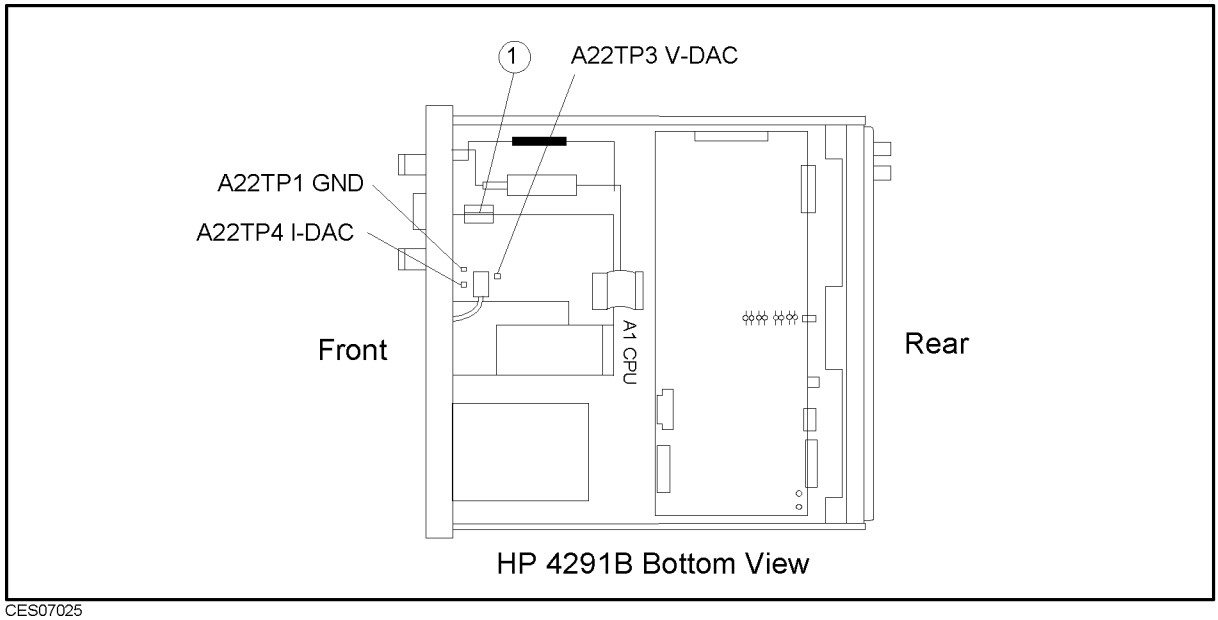


Figure 7-25. A22 Output Voltages Check Location

b. Turn the HP 4291B on. Then press the following keys to set DC bias voltage to 0 V. (Source), BIAS on OFF, (then the label changes to BIAS ON off), DC BIAS MENU, BIAS VOLTAGE, (0), (x1)

c. Change the DC bias voltage settings and check that the A22TP3 (V-DAC) voltage from A22TP1(GND) is within the limits shown in Table 7-4. See Figure 7-25 for the test point locations.

- If the voltage is good, continue with the next step.
- If the voltage is bad, A22 is faulty. Replace A22.

Table 7-4.

Bias Setting	TP3 Voltage Limit
0 V	0 V ±10 mV
4 V	400 mV ±20 mV
10 V	1 V ±50 mV
40 V	4 V ±0.2 V
−4 V	−400 mV ± 20 mV

d. Press the following keys to set DC bias current to 0 A. (Source), BIAS SRC [VOLTAGE], (then the label changes to BIAS SRC [CURRENT]), BIAS CURRENT, (0), (x1)

e. Change the DC bias current settings and check that the A22TP4 (I-DAC) voltage from A22TP1(GND) is within the limits shown in Table 7-5. See Figure 7-25 for the test pin location.

- If the voltage is good, continue with the next step.
- If the voltage is bad, A22 is faulty. Replace A22.

Table 7-5.

Bias Setting	TP4 Voltage Limit
0 A	0 V ±10 mV
10 mA	−556 mV ±56 mV
100 mA	−5.56 V ±0.56 V

f. Press the following keys to check the DC bias gain control circuit operation (DC bias gain is determined using a GAIN DAC). (Source), BIAS SRC [CURRENT], (then the label changes to BIAS SRC [VOLTAGE]), BIAS VOLTAGE, (4), (0), (x1),

(System), SVC MODE, DC BIAS, DC BIAS AUTO man, (then the label changes to DC BIAS auto MAN), DAC, GAINDAC AUTO man, (then the label changes to GAINDAC auto MAN)

g. Press the following keys to set the GAIN DAC value to 0. GAINDAC VALUE, (0), (x1)

h. Measure the A22TP3 voltage from A22TP1, and note the measured value. See Figure 7-25 for the test pin location.

i. Change the GAIN DAC value to 255 using numeric keys.

j. Measure the A22TP3 voltage from A22TP1, and check that the voltage increases by 80 ± 20 mV compared with the voltage noted in step *h*.

- If the voltage is good, A22 is verified and A23 should be faulty. Replace A23.
- If the voltage is bad, A22 is faulty. Replace A22.

CHECK THE A60 HIGH STABILITY FREQUENCY REFERENCE

Perform the following procedures to verify the A60 High Stability Frequency Reference:

1. Observe the REF OVEN signal on the rear panel using a spectrum analyzer. Check that the frequency is 10 MHz and the level is approximately 0 dBm.
   - If the signal is good, continue with the next step.
   - If the signal is bad, inspect the cable and connections between A60 and the REF OVEN. If the cable and connections are good, replace the A60 High Stability Frequency Reference.
2. Perform the *10 MHz Reference Oscillator Frequency Adjustment (Option 1D5 Only).* For the procedure, see Chapter 3.
   - If the adjustment is successfully completed, the A60 High Stability Frequency Reference is verified.
   - If the adjustment fails, check the CAL OUT Signal and the EXT REF operation in accordance with the procedures provided in the *Check A5 Synthesizer Outputs* section of this chapter. If both are good, the A60 High Stability Frequency Reference is probably faulty. Replace A60.

8

Receiver Troubleshooting

INTRODUCTION

Use these procedures only if you have read Chapter 4 and you believe the problem is in the receiver group.

This chapter provides procedures to isolate the faulty assembly in the receiver group.

The procedures isolate the faulty assembly by using the HP 4291B self-test functions (external tests). Remember that these tests are done on the assumption that the source group is operating correctly.

The receiver group consists of the following two assemblies:

- A4A2 Receiver RF (Part of A4 First LO/Receiver RF)
- A6 Receiver IF

Note

Make sure all of the assemblies listed above are firmly seated before performing the procedures in this chapter.

Allow the analyzer to warm up for at least 30 minutes before you perform any procedure in this chapter.

Figure 8-1 is a receiver group simplified block diagram. For more information about circuit operation, see Chapter 11.

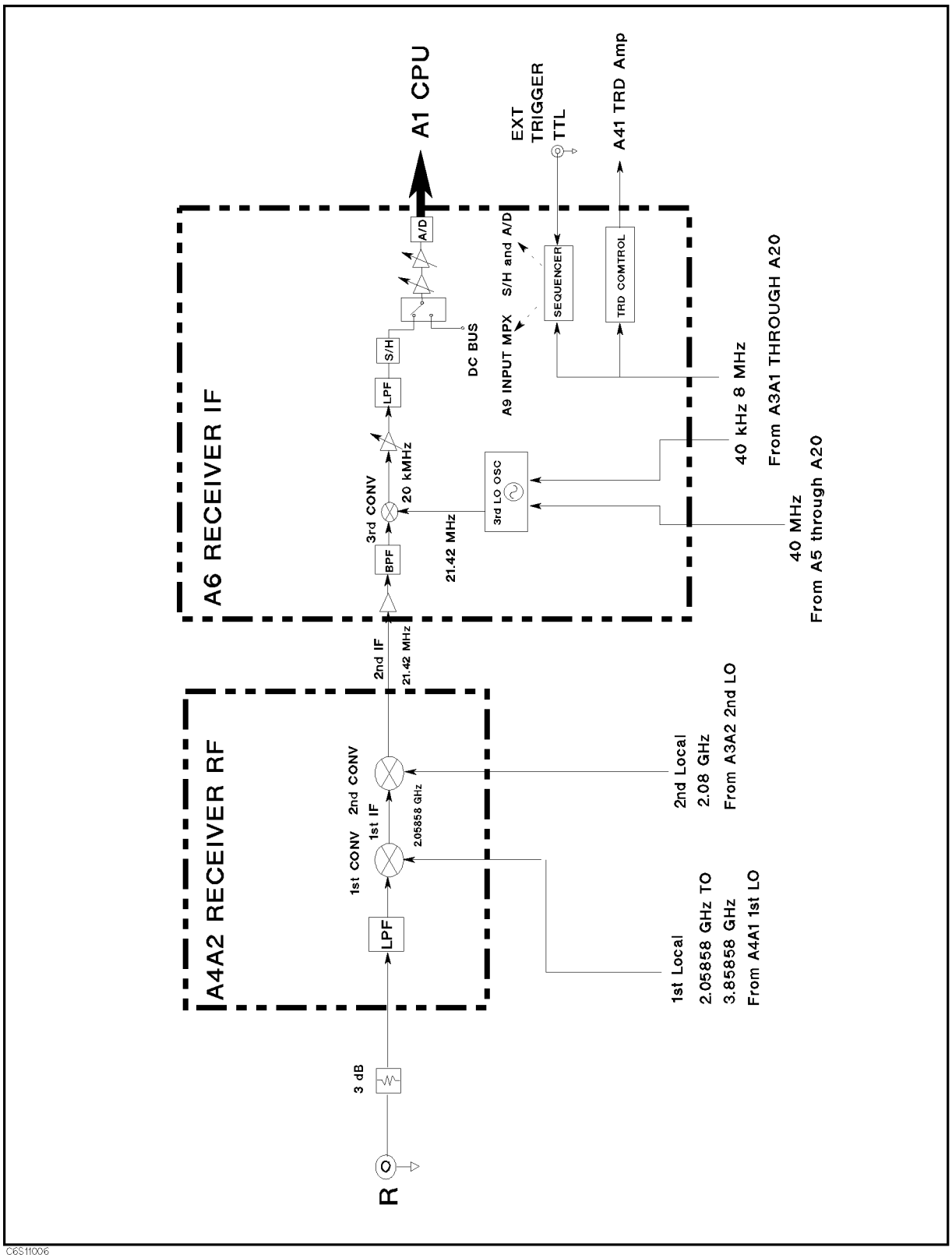


Figure 8-1. Receiver Group Block Diagram

RECEIVER GROUP TROUBLESHOOTING SUMMARY

This section summarizes the troubleshooting sequence in this chapter.

The receiver group troubleshooting flow is shown in Figure 8-2.

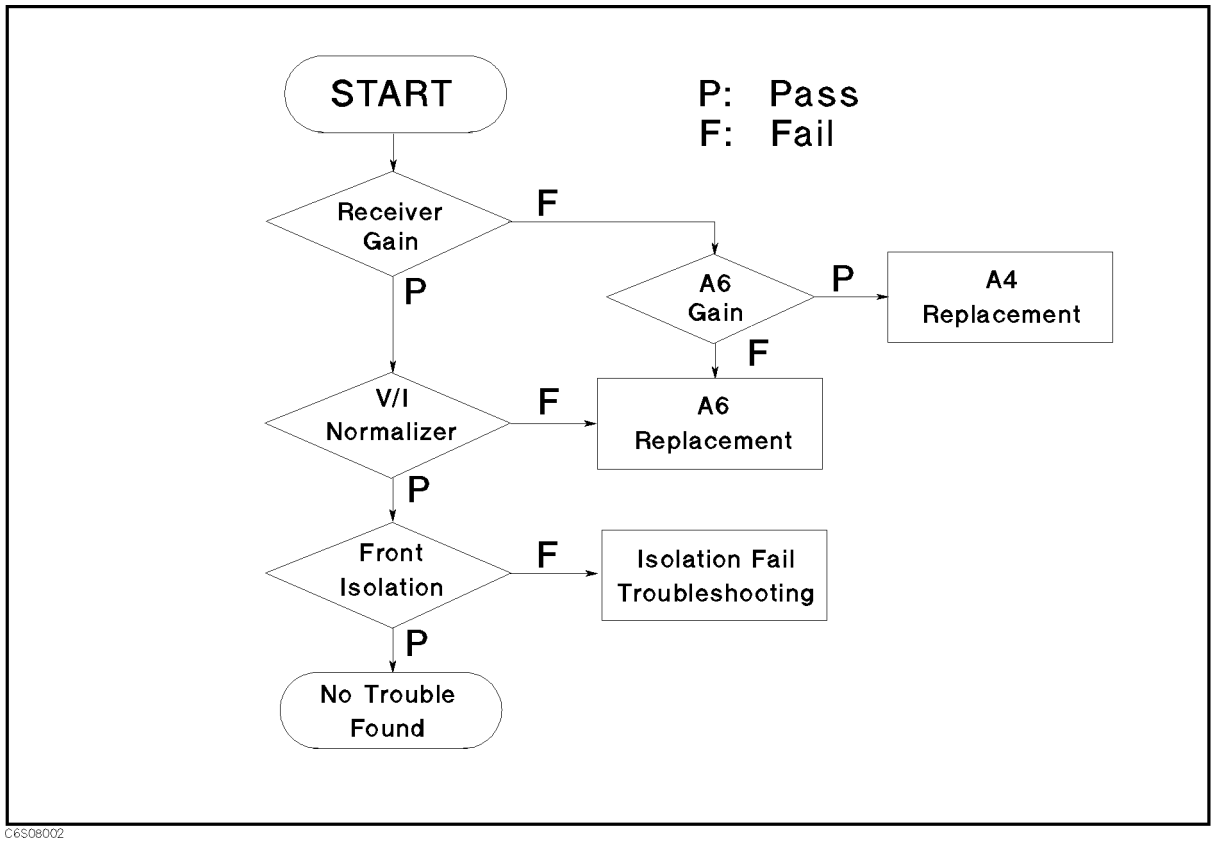


Figure 8-2. Receiver Group Troubleshooting Flow

Troubleshooting consists of two parts. The first part is to isolate the fault between the A4A2 receiver RF and A6 receiver IF. The second part is to verify signal isolation between the source circuits and the receiver circuits.

Fault isolation between A4A2 and A6 is done by using the following three self-tests:

Test Number	Description
22	RECEIVER GAIN
23	A6 GAIN
24	V/I NORMALIZER

After both the RECEIVER GAIN test and V/I NORMALIZER test pass, signal isolation between the source circuits and the receiver circuits is verified using the FRONT ISOL'N test. If the test passes, the receiver group is probably operating correctly.

START HERE

This section provides the step by step troubleshooting procedure using the HP 4291B self-test functions (external tests). For detailed information about the self-test functions, see Chapter 10.

Test Equipment

Type-N Cable, 61 cm .....HP 11500B or part of HP 11851B

Procedure

1. Press (Preset), (System), SERVICE MENUS, TESTS, (2), (2), (x1) to access the RECEIVER GAIN test. When "RECEIVER GAIN" is displayed, press EXECUTE TEST.
2. Perform the test according to the displayed instructions.
   - If the test passes, go to step 7.
   - If the test fails, continue with the next step.
3. Turn the analyzer power off. Remove the "D" cable from the A3A1 ALC out connector, remove the "M" cable from the A4A2 second IF connector, then connect the "M" cable to the A3A1 ALC out connector. The connector locations are shown in Figure 8-3.

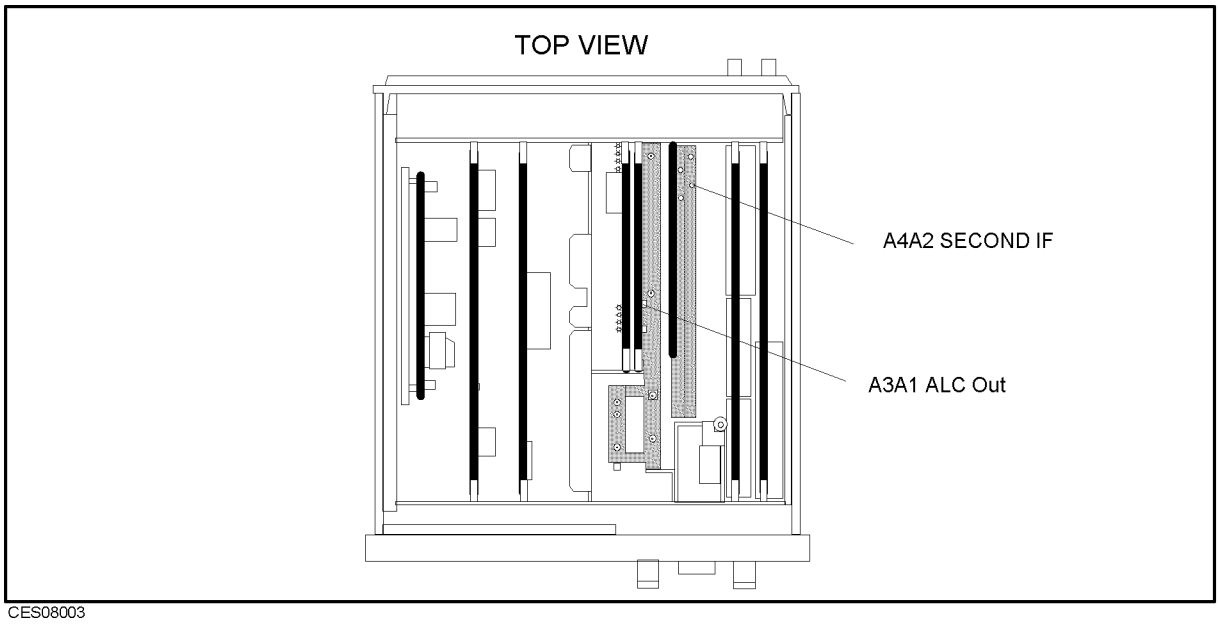


Figure 8-3. A6 GAIN Test Location

4. Turn the analyzer power on.
5. Press (System), SERVICE MENUS, TESTS, (2), (3), (x1) to access the A6 GAIN test. When "A6 GAIN" is displayed, press EXECUTE TEST.
6. Perform the test according to the displayed instructions.
   - If the test passes, reconnect the cables and replace the A4 First LO/Receiver RF.
   - If the test fails, replace the A6 receiver IF and reconnect the cables.

7. Press (↑) twice to access the FRONT ISOL'N test. When "FRONT ISOL'N" is displayed, press EXECUTE TEST .

8. Perform the test according to the displayed instructions.
   - If the test passes, the receiver group is probably operating correctly.
   - If the test fails, go to the *FRONT ISOL'N Test Failure Troubleshooting* procedure.

FRONT ISOL'N Test Failure Troubleshooting

In the FRONT ISOL'N test, the receiver gain is tested first. Then the isolation between the front S and R connectors is tested. Troubleshoot the analyzer as follows when this test fails:

- When "RECEIVER GAIN OUT OF SPEC" appears, confirm the connection between S and R connectors, and perform the test. If the test still fails, replace the A4 First LO/Receiver RF.
- When "FRONT ISOL'N TEST FAILED" appears, check the connectors and semi-rigid cables connected to A3 and A4. Loose connectors and cracked cables can affect the isolation.

9

Transducer Troubleshooting

INTRODUCTION

This chapter provides procedures to isolate the faulty assembly in the transducer group.

Use these procedures only if you have read Chapter 4 and you believe the problem is in the transducer group.

The procedures isolate the faulty assembly by using the HP 4291B self-test functions (external tests). Remember that these tests are done on the assumption that the source group and receiver group are operating correctly.

The transducer group consists of the following assemblies:

- Test Station
- High Impedance Test Head (except Option 011)
- Low Impedance Test Head (Option 012)
- High Temperature High Impedance Test Head (Option 013)
- High Temperature Low Impedance Test Head (Option 014)

Note

Make sure all of the assemblies listed above are firmly seated before performing the procedures in this chapter.

Allow the analyzer to warm up for at least 30 minutes before you perform any procedure in this chapter.

Figure 9-1 and Figure 9-2 are transducer group simplified block diagrams. For more information about the circuit operation, see Chapter 11.

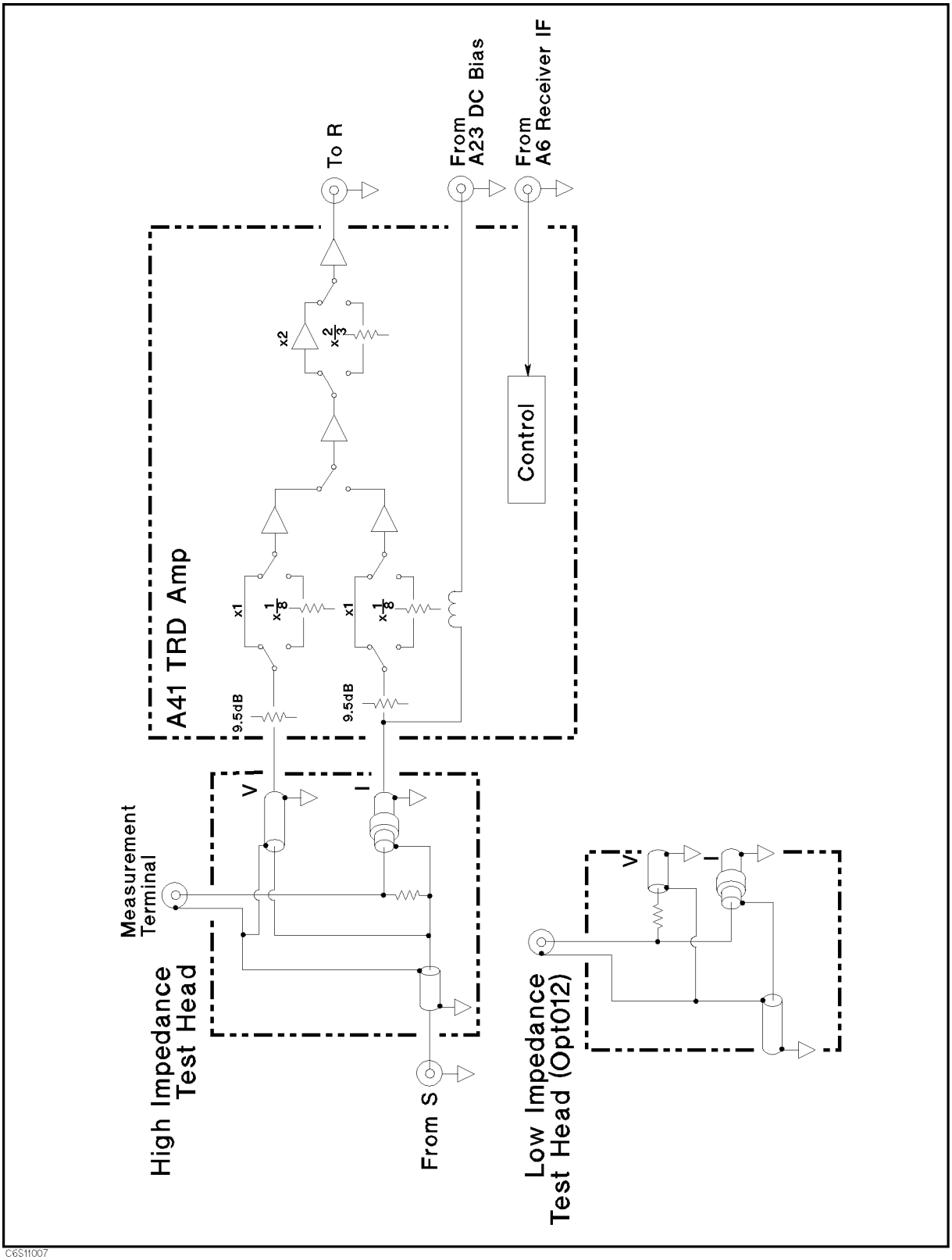
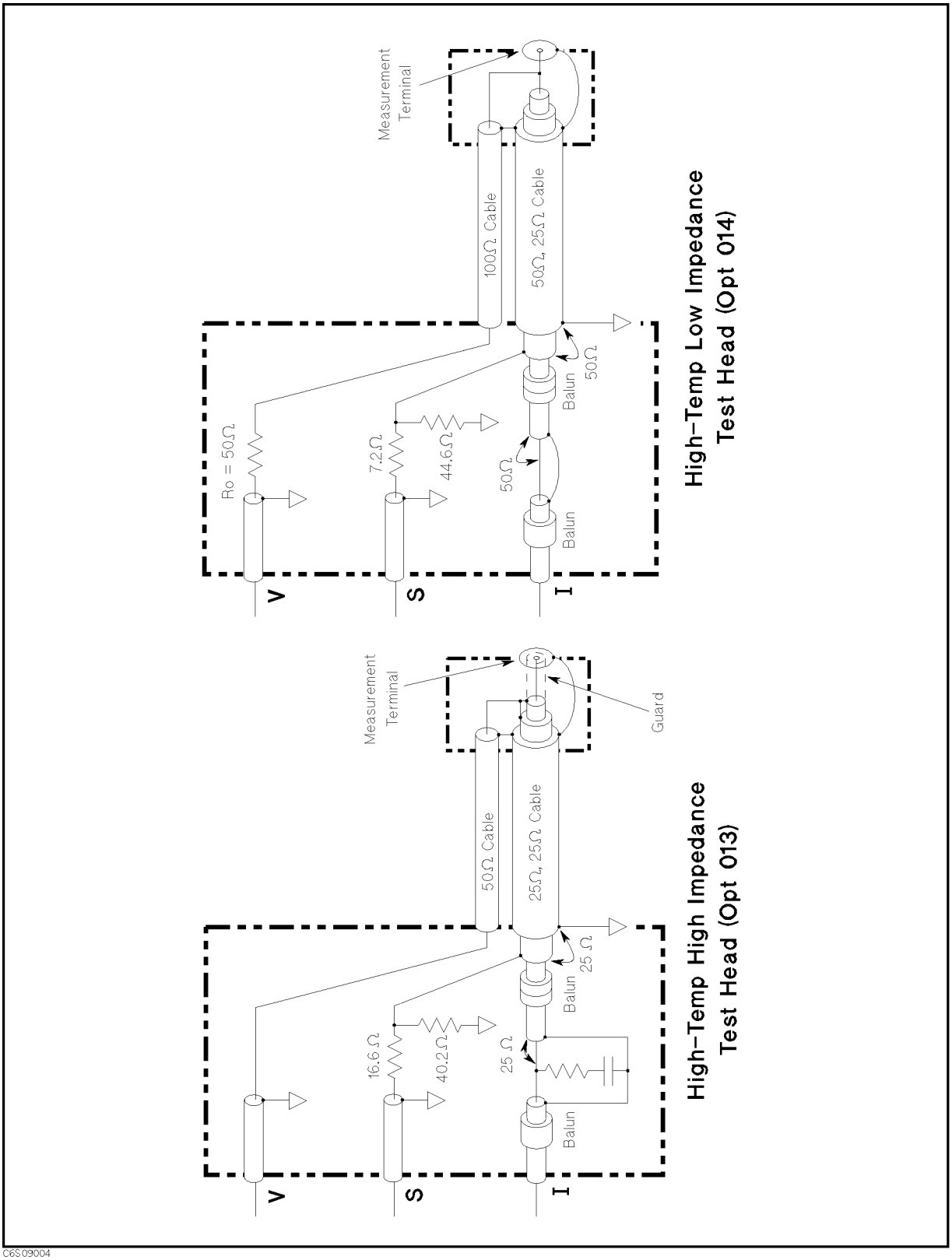


Figure 9-1. Transducer Group Block Diagram (1 of 2)



C6S09004

Figure 9-2. Transducer Group Block Diagram (2 of 2)

TRANSDUCER GROUP TROUBLESHOOTING SUMMARY

This section summarizes the troubleshooting sequence in this chapter.

The transducer group troubleshooting flow is shown in Figure 9-3.

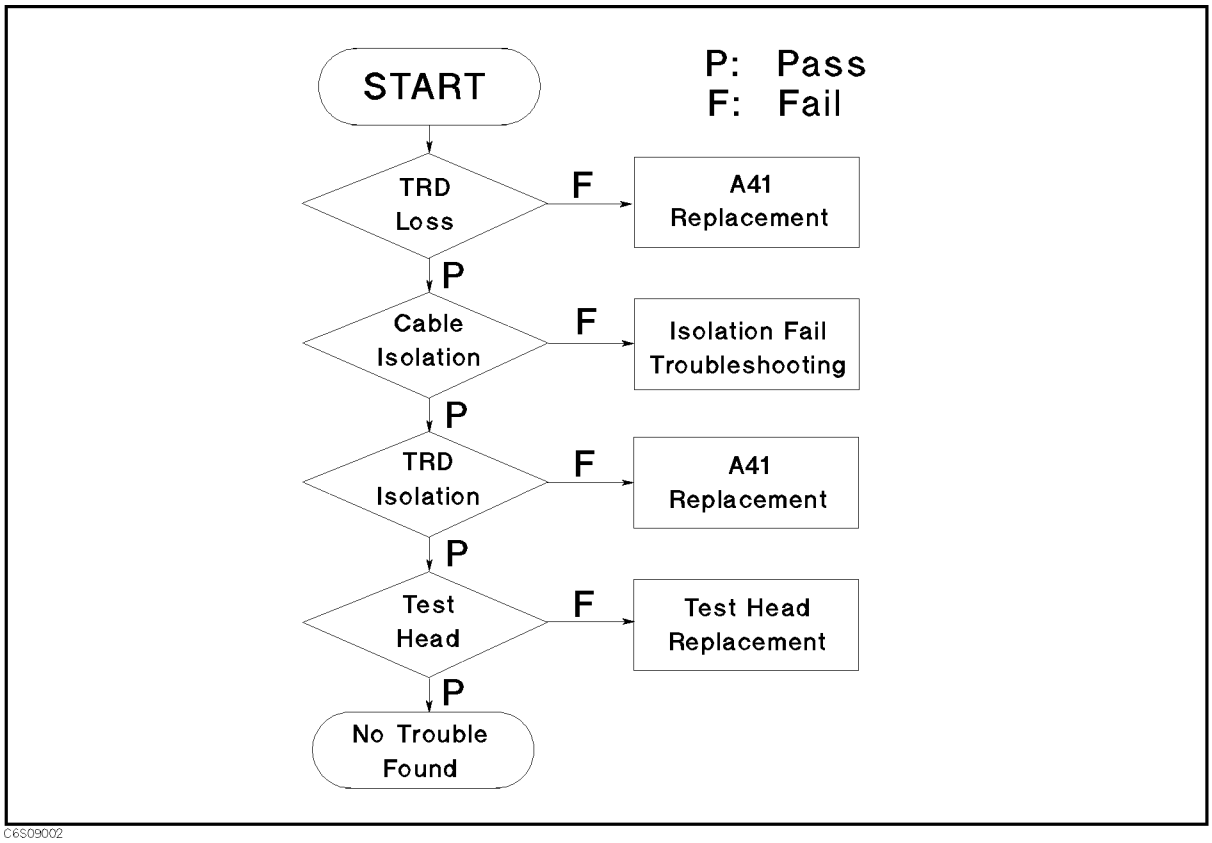


Figure 9-3. Transducer Group Troubleshooting Flow

START HERE

This section provides the step by step troubleshooting procedure using the HP 4291B self-test functions (external tests). For detailed information about the self-test functions, see Chapter 10.

Test Equipment

Type-N Cable, 61 cm ..... HP 11500B or part of HP 11851B
TRD Cable 04291-65001

Procedure

1. Press (Preset), (System), SERVICE MENUS, TESTS, (2), (6), (x1) to access the TRANSDUCER LOSS test. When "TRANSDUCER LOSS" is displayed, press EXECUTE TEST.
2. Perform the test according to the displayed instructions. Test station connector locations are shown in Figure 9-4.

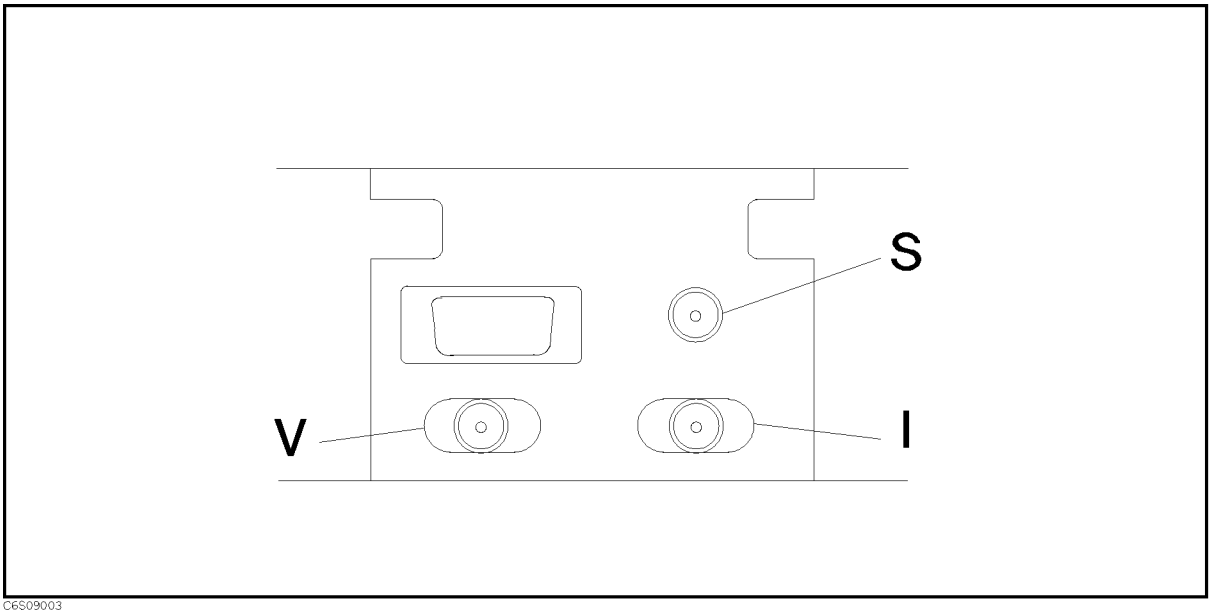


Figure 9-4. Test Station Connectors Locations

- If the test passes, continue with the next step.
- If the test fails, replace the A41 TRD amp.

3. Press (⇧) to access the CABLE ISOL'N test. When "CABLE ISOL'N" is displayed, press EXECUTE TEST.
4. Perform the test according to the displayed instructions.
   - If the test passes, continue with the next step.
   - If the test fails, go to the *CABLE ISOL'N Test Failure Troubleshooting* procedure.
5. Press (⇧) to access the TRD ISOL'N I to V test. When "TRD ISOL'N I to V" is displayed, press EXECUTE TEST.

6. Perform the test according to the displayed instructions. Test station connector locations are shown in Figure 9-4.
   - If the test passes, continue with the next step.
   - If the test fails, replace the A41 TRD amp.
7. Press (↑) to access the TRD ISOL'N V to I test. When "TRD ISOL'N V to I" is displayed, press `EXECUTE TEST`.
8. Perform the test according to the displayed instructions. Test station connector locations are shown in Figure 9-4.
   - If the test passes, continue with the next step.
   - If the test fails, replace the A41 TRD amp.

Note

The HP 4291B has the following four test heads (including the optional heads):

- High impedance test head (except Option 011)
- Low impedance test head (Option 012)
- High temperature high impedance test head (Option 013)
- High temperature low impedance test head (Option 014)

Perform the following steps for all the available test heads.

---

9. Select the test (according to the test head to be verified) using the numeric keys and the (x1) key. Table 9-1 lists the test head tests and applicable test numbers.

Table 9-1. Test Head Tests List

Test Number	Test Name
30	HI Z HEAD
31	LO Z HEAD
32	HI TEMP HI Z HEAD
33	HI TEMP LO Z HEAD

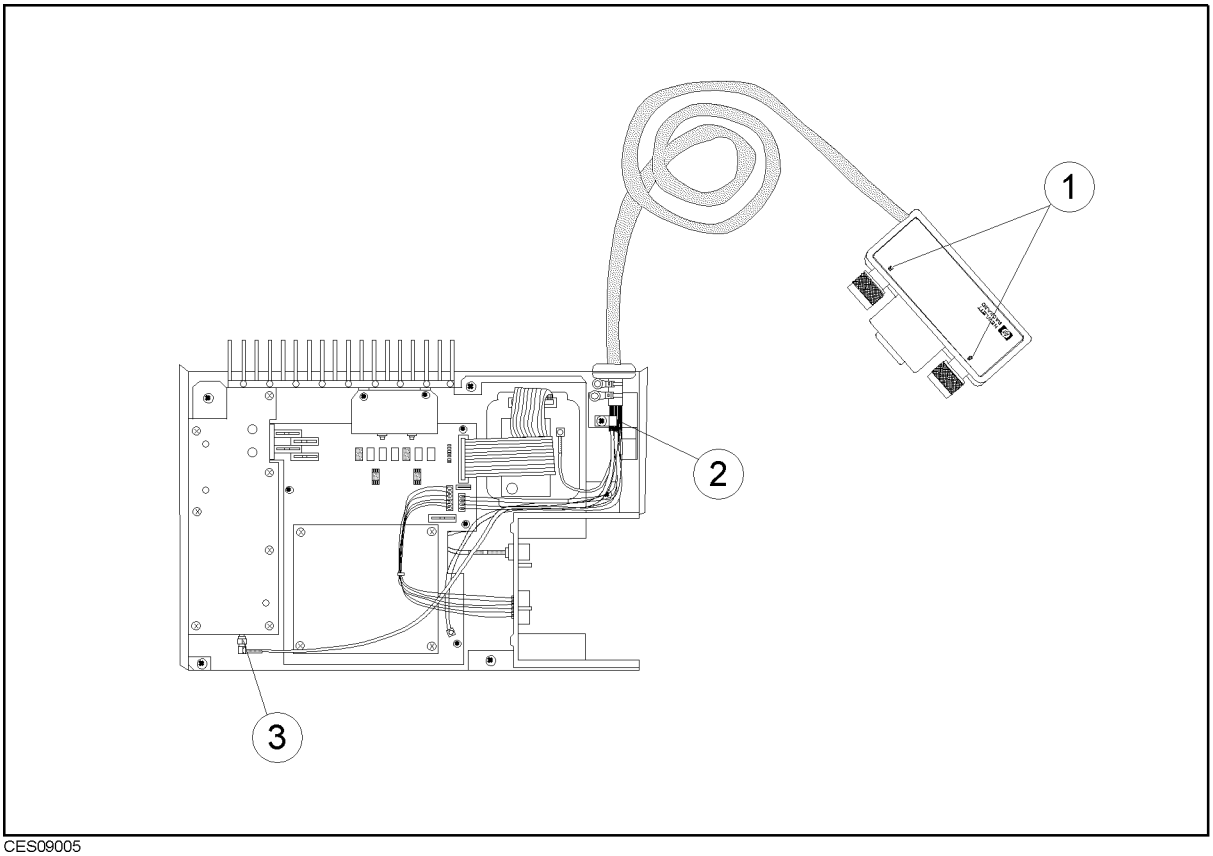
10. Press `EXECUTE TEST` and perform the test according to the displayed instructions. Test station connector locations are shown in Figure 9-4.
    - If the test is passed, perform the test for the other available test heads in the same manner. If all the tests pass, the analyzer is probably operating correctly.
    - If a test fails on test number 30 or 31, visually inspect the test heads 7 mm connector and calibration kit. Troubleshoot them if necessary. If the 7 mm connector and calibration kit are correct and the test still fails, replace the test head.
    - If a test fails on test number 32 or 33, go to the *High Temperature Test Head Trouble Isolation* procedure.

CABLE ISOL'N Test Failure Troubleshooting

In the CABLE ISOL'N test, the receiver gain is tested first. Then the isolation between the test station connectors is tested. When the CABLE ISOL'N test fails, troubleshoot the analyzer as follows:

- When "RECEIVER GAIN OUT OF SPEC" is displayed, confirm the connection between the S and R connectors and reperform the test. If the test still fails, replace the A4 First LO/Transducer RF.

- When “CABLE ISOL’N TEST FAILED” is displayed, confirm the connection between the test station and the mainframe and reperform the test. If the test still fails, confirm the connections shown in Figure 9-5, and reperform the test. If the test still fails, replace the test station cable.



CES09005

Figure 9-5. Cable Isolation Check Points

High Temperature Test Head Trouble Isolation (Opt. 013 and 014)

If the test numbers 32 or 33 fail, perform the following trouble isolation procedures.

High-Z Test Head (Opt. 013)

1. Visually inspect the test head’s 7 mm connector and three connectors to be connected to the test station.
   - If the connector is good, continue with the next step.
   - If the connector is bad, replace the connector.
2. Connect SHORT standard to the 7 mm connector.
3. Measure the test head impedance by pressing (Preset), (Marker→), and enter desired frequency.
   - If the measurement value is greater than 1 kΩ at 1 MHz, I-ch contact may be bad.
   - If the measurement value is almost 25 Ω at all frequencies, V-ch contact may be bad.
   - If the measurement value is unstable and has much noise, S-ch contact may be bad.
4. Connect OPEN standard to the 7 mm connector.

5. Measure the test head admittance by pressing (Meas), MORE 1/5, ADMITTNCE: MAG(|Y|).
   - If the measurement data around 1 MHz is unstable, it is possible that the guard conductor in the triaxial cable is shorting to the ground conductor of the cable in the test head.

Low-Z Test Head (Opt. 014)

1. Visually inspect the test head's 7 mm connector and three connectors to be connected to the test station.
   - If the connector is good, continue with the next step.
   - If the connector is bad, replace the connector.
2. Connect OPEN standard to the 7 mm connector.
3. Measure the test head impedance by pressing (Preset), (Marker→), and enter desired frequency.
   - If the measurement value is almost 100 Ω at all frequencies, I-ch contact may be bad.
   - If the measurement value is less than 50 Ω at 1 MHz, V-ch contact may be bad.
   - If the measurement value is unstable and has much noise, S-ch contact may be bad.
4. Connect SHORT standard to the 7 mm connector.
   - If the measurement data around 1 MHz is unstable, it is possible that the guard conductor in the triaxial cable is shorting to the ground conductor of the cable in the test head.

10

Service Key Menus

INTRODUCTION

The service key menus are used to test, verify, adjust, and troubleshoot the analyzer. They are also used to install and update the firmware in the analyzer.

The service key menus consist of several menus that are accessed through the service menu and the Bootloader menu as shown in Figure 10-1. The service menu is displayed by pressing (System), SERVICE MENU. The Bootloader menu is displayed by turning the analyzer power on while pressing (Preset).

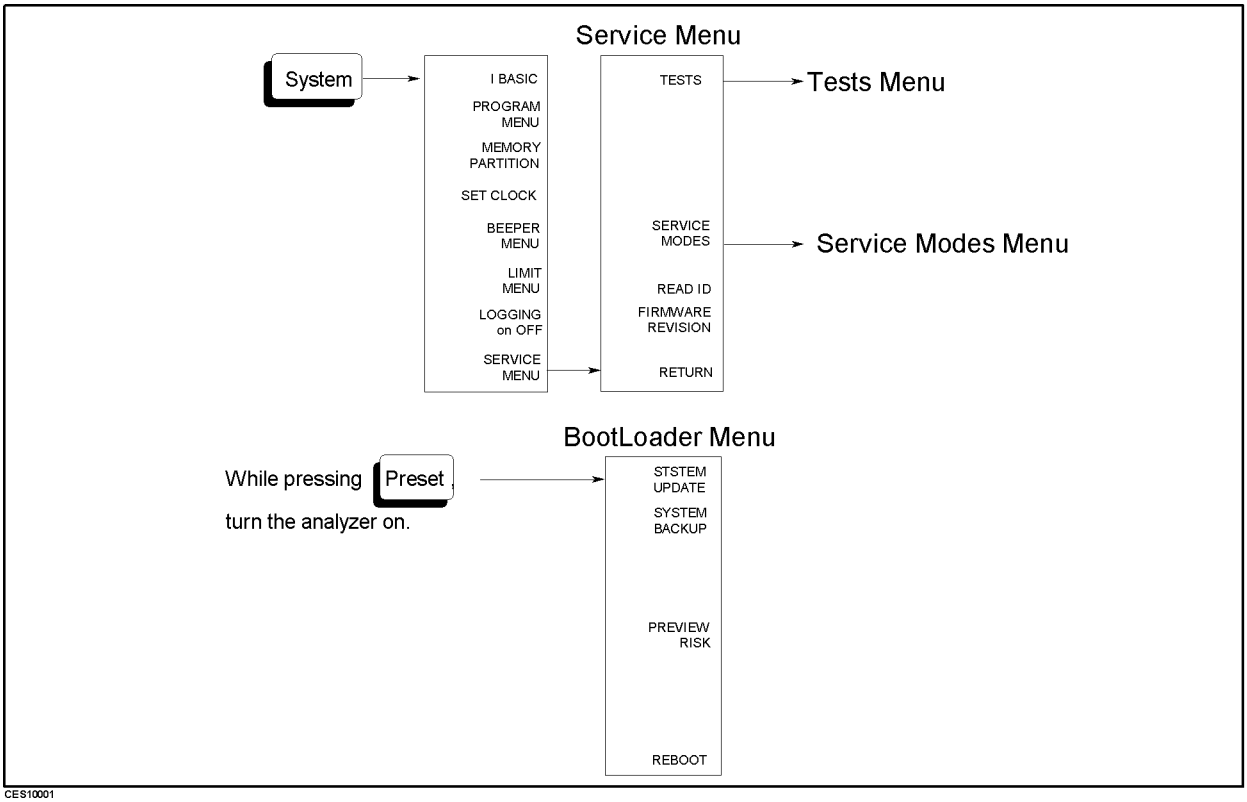


Figure 10-1. Service Key Menus

The service key menus allow you to perform the following functions:

- Select and execute a built-in diagnostic test. The analyzer has 45 built-in diagnostic tests. For detailed information, see the *Tests Menu* in this chapter.
- Control and monitor various circuits for troubleshooting. For detailed information, see the *Service Modes Menu* in this chapter.
- Display which test station and test head are connected.

- Display the firmware revision. See the *Service Menu* in this chapter.
- Install and update the firmware in the analyzer. For detailed information, see the *Bootloader Menu* in this chapter.

When applicable, the HP-IB mnemonic is written in parentheses following the softkey using the following symbol conventions:

{ }	A necessary appendage
<*numeric*>	A necessary numerical appendage
|	A delimiter for applicable appendages. For example, {OFF|ON|0,1|} means OFF, ON, 0, or 1.

For more about the HP-IB commands general information, see the *HP 4291B Programming Manual* .

SERVICE MENU

Figure 10-2 shows the service menu. This menu is used to display the tests menu, the service modes menu, and the firmware revision information. To display the service menu, press (System), SERVICE MENU. Each softkey in the service menu is described below.

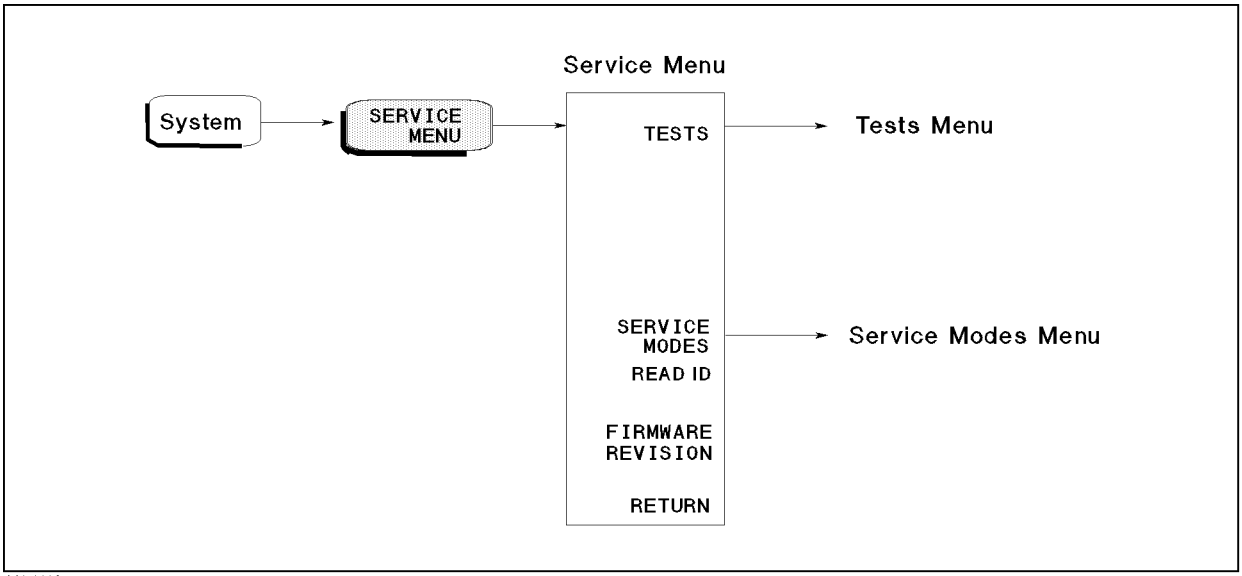


Figure 10-2. Service Menu

TESTS

Displays the tests menu. For more information about the tests menu, see the *Tests Menu* later in this chapter.

SERVICE MODES (:DIAG:SERV:MODE {ON|1})

Activates the service modes and displays the service modes menu. For more information about the service modes menu, see the *Service Modes Menu* later in this chapter.

READ ID

Displays which test station and test head are connected.

FIRMWARE REVISION (:DIAG:FREV?)

Displays the current firmware revision information. The number and implementation date appear in the active entry area of the display as shown below. Another way to display the firmware information is to cycle the analyzer power (off then on).

```
HP 4291B REVN.NN MON DD YEAR HH:MM:SS
```

where	N.NN:	Revision Number
	MON DD YEAR	Implementation Date (Month Day Year)
	HH:MM:SS	Implementation Time (Hour:Minute:Second)

TESTS MENU

Figure 10-3 shows the tests menu. The tests menu is used to select and execute one of the 45 built-in diagnostic tests. More information about the diagnostic tests is provided in the *Diagnostic Tests* later in this section. To display the tests menu, press (System), SERVICE MENU, and TESTS.

When entering the tests menu, internal test 0: ALL INT is selected as the default test. The test number, name, and status abbreviation is displayed in the active entry area of the display. See Figure 10-4. For the test status, see Figure 10-4.

The diagnostic tests are numbered from 0 to 44. To select a test, enter the desired test number using the numeric keypad, (⇧), (⇩), RPG knob or HP-IB command (:DIAG:TEST <*numeric*>).

Each softkey in the tests menu is described below.

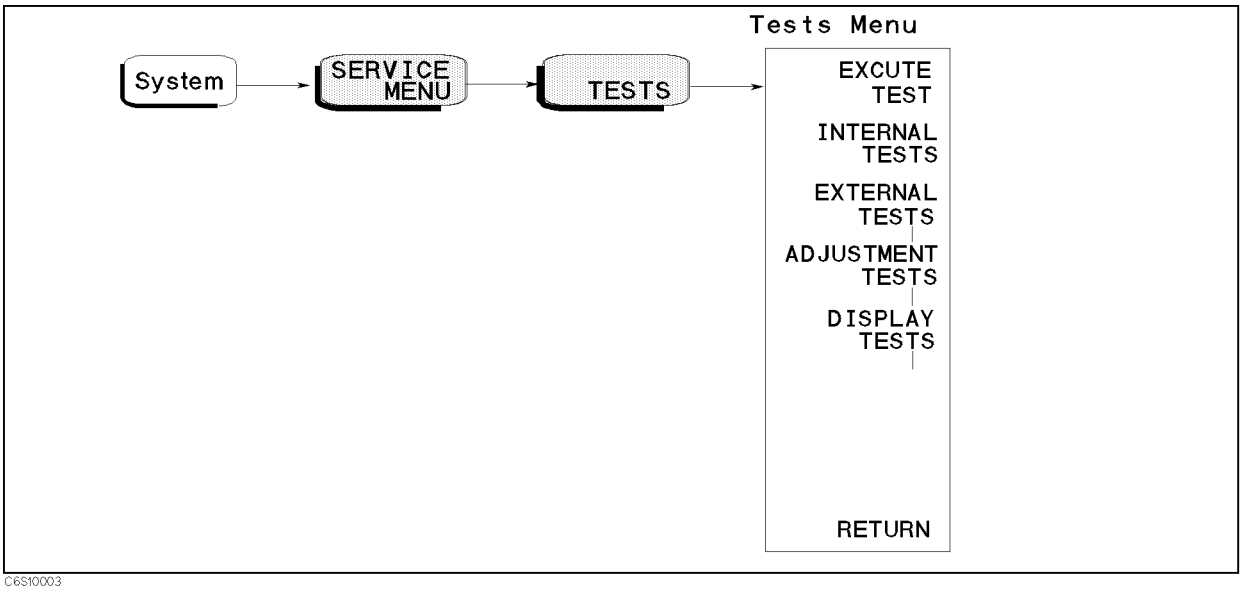


Figure 10-3. Tests Menu

EXECUTE TEST (:DIAG:TEST:EXET)

Runs the selected test. When the executed test requires user interaction, CONT (:DIAG:TEST:CONT) and the instruction appear on the display. Follow the displayed instruction and press CONT to continue the test.

INTERNAL TESTS (:DIAG:TEST 0)

Selects the first internal test 0: ALL INT.

EXTERNAL TESTS (:DIAG:TEST 17)

Selects the first external test 17: FRONT PANEL DIAG.

ADJUSTMENT TESTS (:DIAG:TEST 34)

Selects the first adjustment test 34: HOLD STEP ADJ.

DISPLAY TESTS (:DIAG:TEST 40)

Selects the first display test 40: TEST PATTERN 1.

Note

After executing a test by pressing EXECUTE TEST, an annotation (Svc) is displayed to indicate any tests executed and the analyzer settings changed to the test settings. To return the analyzer to normal operation, cycle the analyzer power (off then on), or press (PRESET).

Note

While any test is being executed, do not change the analyzer setting using the front-panel keys, the HP-IB, or the I-BASIC program. If the setting is changed during test execution, the test result and the analyzer operation are undefined.

Test Status

When selecting a test, the test status abbreviation is displayed as shown in Figure 10-4.

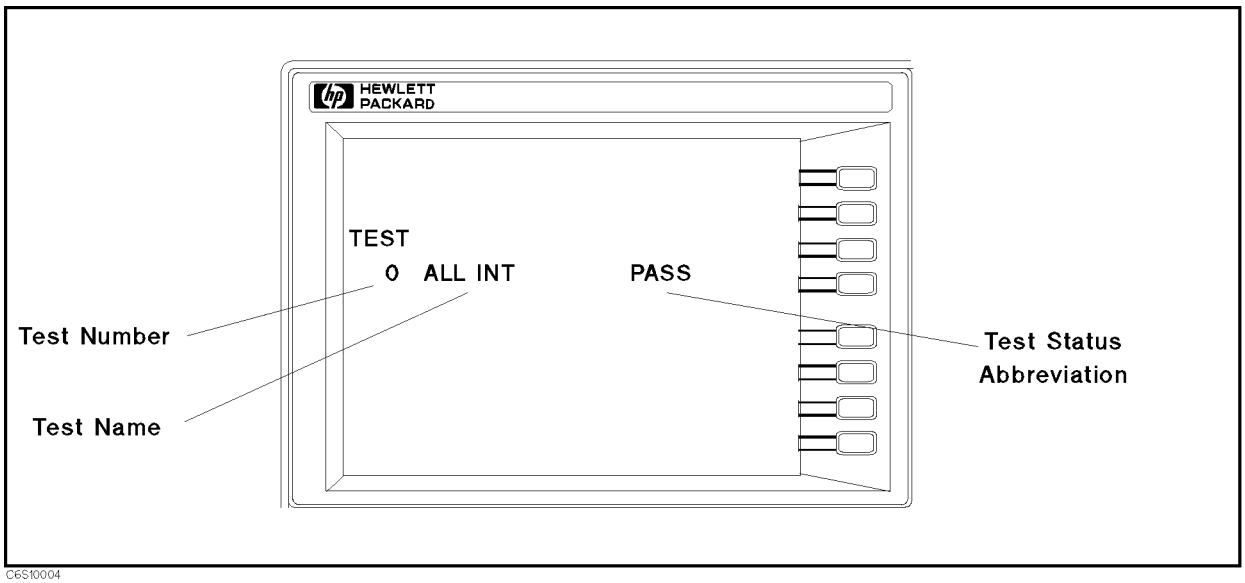


Figure 10-4. Test Status on the Display

To see the test status of the desired test, enter the desired test number using the numeric keypad, (↑), (↓), or RPG knob. Also, the three HP-IB commands listed below are available to get the test status using HP-IB.

`:DIAG:TEST:RES?` <*numeric*>	returns the test status. The <*numeric*> specifies the test number and is an integer from 0 to 44.
`*TST?`	executes internal test 0: ALL INT and returns the test result.
`:DIAG:INIT:RES?`	returns the power on self-test result.

A sample program using the command `:DIAG:TEST:RES?` is as shown below. This program displays the test status of internal test 1. See the *HP 4291B Programming Manual* for more information.

```
10    !
20    ASSIGN @Hp4291 TO 717 ! When IBASIC is used, replace "717" to "800."
30    !
40    OUTPUT @Hp4291;"DIAG:TEST:RES? 1"
50    ENTER @Hp4291;Test_status$
60    PRINT Test_status$
70    !
```

Sample Program Using `:DIAG:TEST:RES?`

Table 10-1 shows the test status abbreviation, its definition, and the HP-IB test status code.

Table 10-1. Test Status Terms

Status Abbreviation	Definition	HP-IB Code
PASS	Pass	"PASS"
FAIL	Fail	"FAIL"
-IP-	In progress	"BUSY"
-ND-	Not done	"NDON"
DONE	Done	"DONE"

The test status is stored in nonvolatile memory (battery backup memory). If the power to the nonvolatile memory is lost, the analyzer will set all test status abbreviations to "-ND-" (not done). If a test is aborted by pressing any key during its execution, the test status is undefined.

Diagnostic Tests

The analyzer has 45 built-in diagnostic tests. The analyzer performs the power on self-test every time the power on sequence occurs (when the analyzer is turned on). These tests are used to test, verify, adjust, and troubleshoot the analyzer.

The 45 built-in diagnostic tests are divided by function into three categories: internal tests, external tests, adjustment tests, and display test. Each group is described below. Descriptions of the tests in each category are given in the *Test Descriptions* section. To access the first test in each category, the category softkey is available in the tests menu.

The power on self-test consists of internal tests 4, 5, 6, 7, and 9 through 16. They are executed in the listed order. If any of the tests fail, that test displays a "`POWER ON TEST FAILED`" message at the end of the power on sequence. The first failed test indicates the most probable faulty assembly.

Internal Test	These tests are completely internal and self-evaluating. They do not require external connections or user interaction. The analyzer has 16 internal tests.
External Tests	These are additional self-evaluating tests. However, these tests require some user interaction (such as key entries). The analyzer has 17 external tests.
Adjustment Tests	These tests are used to adjust the analyzer. See the *Adjustments and Correction Constants* chapter. The analyzer has 7 adjustment tests.
Display Tests	These tests are used to adjust and check for proper operation of the display circuits. The analyzer has 5 display tests.

Test Descriptions

This section describes all 45 diagnostic tests.

`INTERNAL TESTS`

This group of tests run without external connections or operator interaction. All return a "PASS" or "FAIL" indication on the display. Except as noted, all are run during the power on self-test and when (Preset) is pressed.

0: ALL INT

Runs only when selected. It consists of internal tests 1 and 4 through 16. If any of these tests fail, this test displays the "FAIL" status indication. Use the RPG knob to scroll through the tests to see which test failed. If all pass, the test displays the "PASS" status indication. Each test in the subset retains its own test status.

1: A1 CPU

Verifies the following circuit blocks on the A1 CPU:

- Digital Signal Processor (DSP)
- System Timer
- Real Time Clock
- Front Key Controller
- Flexible Disk Drive Controller
- HP-IB Controller
- EEPROM

2: A1 VOLATILE MEMORY

Runs only when selected. It verifies the A1 volatile memories:

CPU internal SRAM
DSP SRAM
Dual Port SRAM
Backup SRAM

At the end of the test, the analyzer is set to the power-on default state because the data in the tested memories is destroyed. During this test, a test pattern is written into the memories and then the pattern is read back and checked.

If the test fails, the test displays an error message for a few seconds and then sets the analyzer to the default state. The error message indicates the faulty memory.

3: A51 GSP

Runs only when selected. It verifies the following circuit blocks on the A51 GSP:

GSP Chip
DRAM
VRAM

When this test starts, Ch 1 LED and Ch 2 LED are turned off. At the end of this test, the analyzer is set to the power-on default state because the data in the tested memories is destroyed. During this test, a test pattern is written into the memories and then the pattern is read back and checked.

If the test fails, the test indicates the faulty circuit using the Ch 1 LED, the Ch 2 LED, and beeps. It then sets the analyzer to the default state. If the GSP chip is faulty, a beep sounds and the LEDs blink once. If the DRAM is faulty, two beeps sound and the LEDs blink twice. If the VRAM is faulty, three beeps sound and the LEDs blink three times.

4: A2 POST REGULATOR

Verifies all A2 post regulator output voltages:

+5 V(AUX), +15 V(AUX)
−15 V, −12.6 V, −5 V, +5 V, +5.3 V, +8.5V, +15 V, +22 V, FAN POWER, GND

This test measures the A2 output voltages at DC bus nodes 1 through 12, and 26. It checks that each measured value is within limits.

5: A6 A/D CONVERTER

Verifies the following circuit blocks on the A6 Receiver IF:

A/D Converter
Gain Y
Gain Z
Range R

This test measures the A/D converter's reference voltage (VREF) at DC bus node 25 through the gain Y, the gain Z, and the range R. These circuits are set to several settings in the test. For each setting, this test checks that the measured value is within limits.

6: A5 REFERENCE OSC

Verifies the reference oscillator in the A5 synthesizer. This test measures the VCO tuning voltage at DC bus node 22 and the frequency (2.5 MHz) at frequency bus node 6. It then checks that each measured value is within limits.

7: A5 FRACTIONAL N OSC

Verifies the fractional N oscillator in the A5 synthesizer. This sets the oscillator frequency to several frequencies over the entire range. For each setting, this test measures the VCO tuning voltage at DC bus node 20 and the frequency at frequency bus node 4. It then checks that each measured value is within limits.

8: A5 STEP OSC

Runs only when selected. It verifies the step oscillator in the A5 synthesizer. This test sets the oscillator frequency to several frequencies over the entire range. For each frequency, the test measures the VCO tuning voltage at DC bus node 19 and the frequency at frequency bus node 3. It then checks that each measured value is within limits.

9: A4A1 1ST LO OSC

Verifies the 1st LO oscillator in the A4A1 1st LO. This test sets the oscillator frequency to several frequencies over the entire range. For each frequency, the test measures the VCO tuning voltage at DC bus node 18 and checks that each measured value is within limits.

10: A3A2 2ND LO OSC

Verifies the 2nd LO oscillator in the A3A2 2nd LO. This test measures the VCO tuning voltage at DC bus node 14 and checks that the measured value is within limits.

11: A3A1 DIVIDER

Verifies the divider circuit in the A3A1 Source Vernier. This test measures the frequency (40 kHz) at frequency bus node 2 and checks that the measured value is within limits.

12: A6 3RD LO OSC

Verifies the 3rd LO oscillator on the A6 receiver IF. This test measures the VCXO tuning voltage at DC bus node 23 and the frequency (40 kHz) at frequency bus node 6. It then checks that each measured value is within limits.

13: A3A1 SOURCE OSC

Verifies the source oscillator in the A3A1 Source Vernier. This test measures the VCXO tuning voltage at DC bus node 13 and the frequency (40 kHz) at frequency bus node 1. It then checks that each measured value is within limits.

14: A6 SEQUENCER

Verifies the A/D sequencer circuit in the A6 receiver IF. This test measures the frequency (80 kHz) of the A/D sequence output at frequency bus node 7 and checks that the measured value is within limits.

15: SOURCE LEVEL

Verifies the source circuit. This test measures the A3A3 output at DC bus node 15 in A3A1. It then checks that each measured value is within limits.

16: DC BIAS

Verifies the A22 and A23 DC bias circuit. This test measures A23 output at DC bus node 26 and 27. It then checks that each measured value is within limits.

`EXTERNAL TESTS`

This group of tests require either external equipment and connections or operator interaction to run. These tests are used in the *Troubleshooting* chapter.

17: FRONT PANEL DIAG.

Checks the RPG and all front-panel keys on the A30 keyboard. The abbreviated name is displayed when pressing one of the keys or rotating the RPG.

18: DSK DR FAULT ISOL'N

Checks the FDD (Flexible Disk Drive). When this test is started, a bit pattern is written to the flexible disk. Then the pattern is read back and checked. This write pattern check is repeated from the low to high addresses.

Note After this test is performed, the data stored on the floppy disk is lost.

19: POWER SWEEP LINEARITY

Checks that the power sweep linearity is within limits. As a result, A3A1, A3A2 and A3A3 are verified.

The analyzer mainframe "S" and "R" connectors are connected, and the "S" output level is measured at the "R" input.

20: SOURCE FLATNESS

Checks that the source flatness is within limits. As a result, A3A1, A3A2 and A3A3 are verified.

The analyzer mainframe "S" and "R" connectors are connected, and the "S" output level is measured at the "R" input.

21: OUTPUT ATTENUATOR

Checks that the A7 attenuation accuracy is within limits. As a result, A7 is verified.

The analyzer mainframe "S" and "R" connectors are connected, and the "S" output level is measured at the "R" input.

22: RECEIVER GAIN

Checks that the receiver circuit gain is within limits. As a result, A4A2 and A6 are verified.

The analyzer mainframe "S" and "R" connectors are connected, and the "R" input gain is tested using the "S" output.

23: A6 GAIN

Checks that the A6 gain is within limits. As are result, A6 is verified.

The A3A1 21.42 MHz output is directly applied to the A6 input.

24: A6 V/I NORMALIZER

Checks that the A6 V/I normalizer (GAIN X, Y, and Z) gain change is within limits. As a result, A6 is verified.

The analyzer mainframe "S" and "R" connectors are connected, and the "R" input gain change is tested using the "S" output.

25: FRONT ISOL'N

Checks that the analyzer mainframe front isolation is sufficient.

The analyzer mainframe "S" and "R" connectors are connected, and the "S" output level is measured at the "R" input. Then the "S" and "R" connectors are disconnected, and the "R" measurement result is compared with the previous measurement result.

26: TRD LOSS

Checks that the analyzer test station loss is within limits. As a result, the test station is verified.

The analyzer mainframe "S" and "R" connectors are connected, and mainframe is calibrated. Then the loss through the test station is measured with the mainframe.

27: CABLE ISOLATION

Checks that the analyzer test station cable isolation is sufficient. As a result, the test station cable is verified.

The analyzer mainframe "S" and "R" connectors are connected, and the "S" output level is measured at the "R" input. Then the test station is connected to the mainframe, and the "R" measurement result is compared with the previous measurement result.

28: TRD ISOL'N I TO V

Checks that the analyzer test station "V" channel isolation when the OSC signal is applied to the "I" channel is sufficient. As a result, the test station is verified.

The analyzer test station "V" channel input is measured while applying the OSC signal to the "I" channel.

29: TRD ISOL'N V TO I

Checks that the analyzer test station "I" channel isolation when the OSC signal is applied to the "V" channel is sufficient. As a result, the test station is verified.

The analyzer test station "I" channel input is measured while applying the OSC signal to the "V" channel.

30: HIGH Z HEAD

Checks that the analyzer high impedance test head characteristics are correct. As a result the test head is verified.

The test station "S" and "V" connectors are connected, and the test station and mainframe are calibrated. Then test head characteristics are verified while connecting the 0 S, 0 Ω, and 50 Ω terminations.

31: LOW Z HEAD

Checks that the analyzer low impedance test head characteristics are correct. As a result the test head is verified.

The test station "S" and "V" connectors are connected, and the test station and mainframe are calibrated. Then test head characteristics are verified while connecting the 0 S, 0 Ω, and 50 Ω terminations.

32: HIGH TEMP HIGH Z HEAD

Checks that the analyzer high temperature high impedance test head characteristics are correct. As a result the test head is verified.

The test station "S" and "V" connectors are connected, and the test station and mainframe are calibrated. Then test head characteristics are verified while connecting the 0 S, 0 Ω, and 50 Ω terminations.

33: HIGH TEMP LOW Z HEAD

Checks that the analyzer high temperature low impedance test head characteristics are correct. As a result the test head is verified.

The test station "S" and "V" connectors are connected, and the test station and mainframe are calibrated. Then test head characteristics are verified while connecting the 0 S, 0 Ω, and 50 Ω terminations.

ADJUSTMENT TESTS

This group of tests is used when adjusting the analyzer. These tests make the adjustment procedure easier. For more detailed operating information, see Chapter 3.

34: HOLD STEP ADJ

Used when the *Hold Step Adjustment* on the A6 receiver IF is performed.

35: BPF ADJ

Used when the *Band Pass Filter Adjustment* on the A6 receiver IF is performed.

36: 3RD VCXO LEVEL ADJ

Used when the *Third Local VCXO Adjustment* on the A6 receiver IF is performed.

37: 2ND LO PLL LOCK ADJ

Used when the *Second Local PLL Lock Adjustment* on the A3A2 2nd LO is performed.

38: SOURCE MIXER LEAK ADJ

Used when the *Source Mixer Local Leakage Adjustment* on the A3A2 2nd LO is performed.

39: SOURCE VCXO LEVEL ADJ

Used when the *Source VCXO Adjustment* on the A3A1 level vernier is performed.

DISPLAY TESTS

These tests are test patterns that are used in the factory for display adjustments, diagnostics, and troubleshooting. They are not used for field service. Test patterns are executed by entering the test number (40 through 44), then pressing EXECUTE TEST, CONTINUE. The test pattern is displayed and the softkey labels are blanked. To exit the test pattern and return to the softkey labels, press softkey 8 (on the bottom). The following is a description of the test patterns.

Note

Do NOT press any keys except softkey 8 (on the bottom) while the test pattern is being executed. If you do, you CANNOT quit the test pattern (that is, you can quit the test pattern only when the analyzer is turned OFF).

40: TEST PATTERN 1

All Black. This pattern is used to verify the color purity of the LCD.

41: TEST PATTERN 2

All White. This pattern is used to verify the color purity of the LCD.

42: TEST PATTERN 3

All Red. This pattern has the same use as TEST PATTERN 2.

43: TEST PATTERN 4

All Green. This pattern has the same use as TEST PATTERN 2.

44: TEST PATTERN 5

All Blue. This pattern has the same use as TEST PATTERN 2.

SERVICE MODES MENU

Figure 10-5 shows the service modes menu. The service modes menu leads to one of the menus used to control the analyzer service modes. For the analyzer's service modes, see the *Service Modes* . To display the service modes menu, press (System), SERVICE MENU, and SERVICE MODES. Each softkey in the service modes menu is described below.

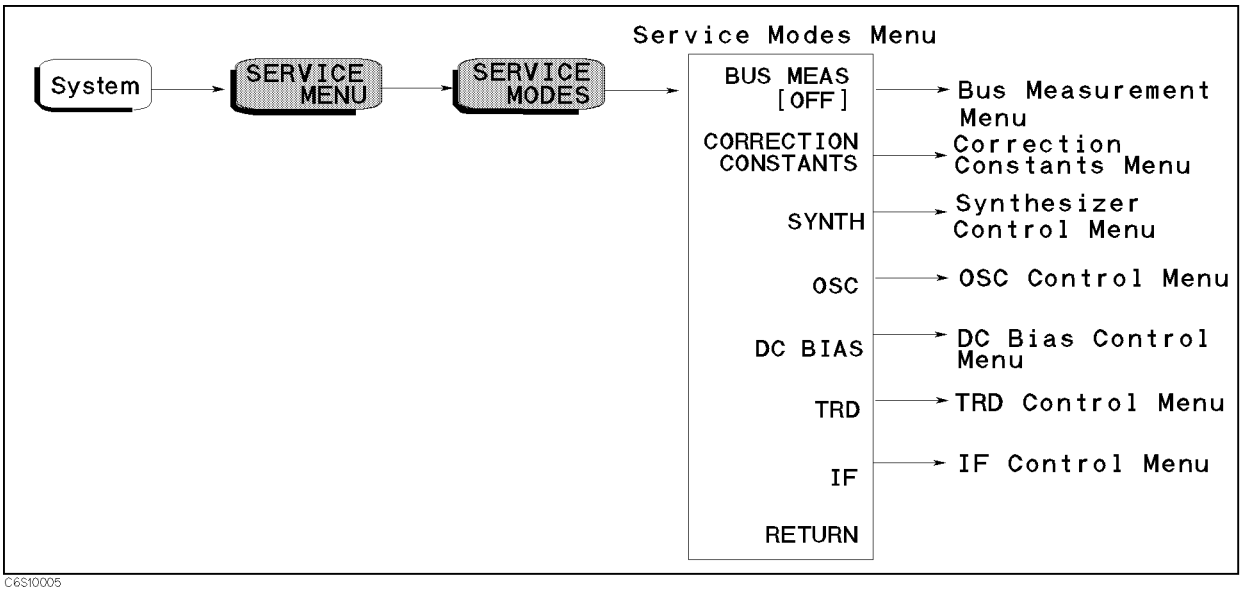


Figure 10-5. Service Modes Menu

BUS MEAS [OFF]

Displays the Bus Measurement Menu. See the *Bus Measurement Menu* in this chapter.

CORRECTION CONSTANTS

Displays the Correction Constant Menu. See the *Correction Constant Menu* in this chapter.

SYNTH

Displays the Synthesizer Control Menu. See the *Synthesizer Control Menu* in this chapter.

OSC

Displays the OSC Control Menu. See the *OSC Control Menu* in this chapter.

DC BIAS

Displays the DC Bias Control Menu. See the *DC Bias Control Menu* in this chapter.

TRD

Displays the Transducer Control Menu. See the *Transducer Control Menu* in this chapter.

IF

Displays the IF Control Menu. See the *IF Control Menu* in this chapter.

Service Modes

The analyzer has various service modes. These service modes are powerful tools to test, verify, adjust, and troubleshoot the analyzer. The service modes are divided by function into the five groups listed below:

Bus Measurement	measures and displays the signal voltage or frequency at the selected bus node of the analyzer. This service mode allows you to check the circuit operation by monitoring the circuit signal without accessing the inside of the analyzer.
Correction Constants On/Off	allows you to turn one (or more) of the corrections on/off.
Synthesizer Control	allows you to control the internal circuit settings in the A5 synthesizer.
OSC Control	allows you to control the internal circuit settings in the A3A1 Source Vernier.
DC Bias Control	allows you to control the internal circuit settings in the A22 and A23 DC Bias.
Transducer Control	allows you to control the internal circuit settings in the A41 TRD Amp.
IF Control	allows you to control the internal circuit settings in the A6 receiver IF.

Note

After pressing SERVICE MODES, an annotation (Svc) is displayed to indicate that the service modes are activated. The settings made in the service modes are kept until the analyzer is turned off or (PRESET) is pressed.

BUS MEASUREMENT MENU

Figure 10-6 shows the bus measurement menu. This menu is used to control the bus measurements. For more information about the bus measurements, see the *Bus Measurement*. For the bus measurement procedure, see the *Bus Measurement Procedure* .

To display the bus measurement menu, press (System), SERVICE MENU, SERVICE MODES, and BUS MEAS [ ]. Each softkey in the bus measurement menu is described below.

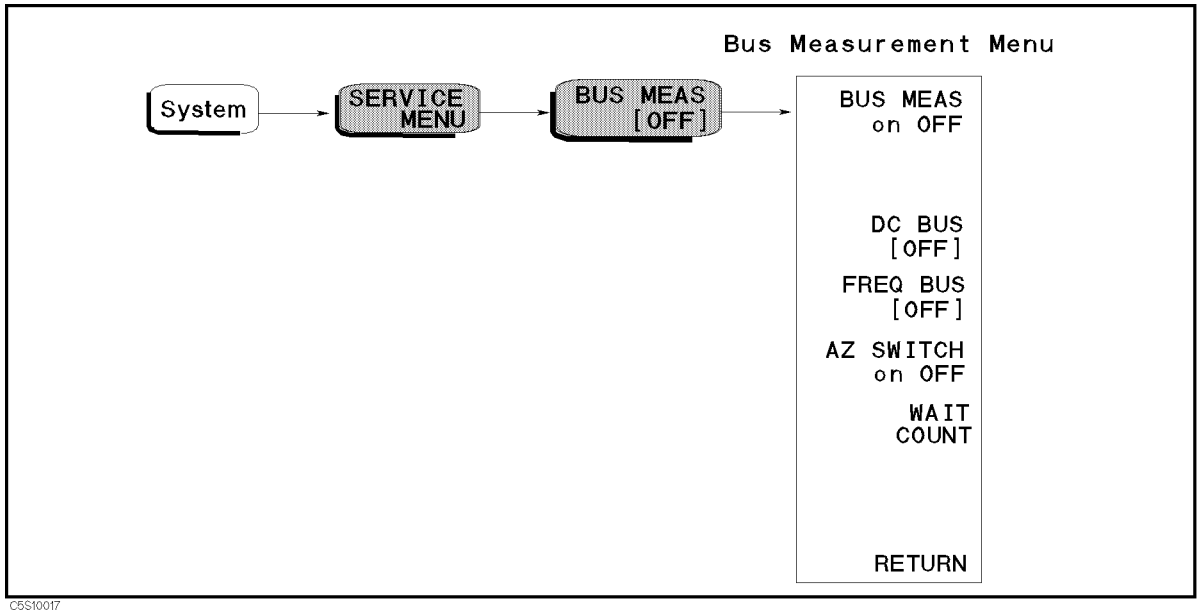


Figure 10-6. Bus Measurement Menu

BUS MEAS on OFF (:DIAG:SERV:BUS:STAT {ON|OFF})

Toggles the bus measurement on and off. After pressing this softkey, the menu changes to BUS MEAS ON off and the measured value of the bus measurement is displayed.

DC BUS [OFF] (:DIAG:SERV:BUS:DC <*numeric*>)

Allows you to select one of the DC bus nodes. The DC bus nodes are numbered from 0 to 29. To select the desired DC bus node, press this softkey and then enter the node number by using the numeric keypad, (↑), (↓), or RPG knob. The node number and name are displayed in the active entry area of the display and the node abbreviation is displayed in the brackets of the menu.

FREQ BUS [OFF] (:DIAG:SERV:BUS:FREQ <*numeric*>)

Allows you to select one of the frequency bus nodes. The frequency bus nodes are numbered from 0 to 7. To select the desired frequency bus node, press this softkey and then enter the frequency node number by using the numeric keypad, (↑), (↓), or RPG knob The node number and name are displayed in the active entry area of the display and the node abbreviation is displayed in the brackets of the menu.

`AZ SWITCH on OFF` (:DIAG:SERV:BUS:AZER {OFF|ON|0|1})

Toggles the auto zero switch on and off.

`WAIT COUNT` (:DIAG:SERV:BUS:WAIT <*numeric*>)

Sets the wait count to specify the wait time in the DC bus measurement. The wait count is an integer from 2 to 32767. When the wait count is N, the analyzer waits N * 12.5 μsec before each DC bus measurement.

Bus Measurement

In this service mode, the analyzer measures and displays the signal voltage or frequency at the selected bus node. This service mode allows you to check the circuit operation by monitoring the circuit signal without accessing the inside of the analyzer.

The analyzer has 36 bus nodes for this service mode. Of these, 29 bus nodes are for DC voltage measurement. These nodes are connected to the A/D converter in the A6 receiver IF through the DC Bus, a single multiplexer line with twenty-nine channels. The other 7 bus nodes are for frequency measurement. These nodes are connected to the frequency bus timer in the A1 CPU through the frequency bus, a single multiplexer line with 7 channel.

Each of the DC bus nodes and the frequency bus nodes is described in the *DC Bus Nodes* and *Frequency Bus Nodes* in this section.

Bus Measurement Procedure

Use this procedure to perform the bus measurement.

1. Press (Preset) to initialize the analyzer.
2. Set the analyzer controls to the settings that you desire to observe in the bus measurement.
3. Press (System), `SERVICE MENU`, `SERVICE MODES`, `BUS MEAS` to display the bus measurement menu.
4. Select the desired bus node as follows:
   - If a DC bus measurement is desired, press `DC BUS [OFF]`. Then enter a node number between 1 and 29.
   - If a frequency bus measurement is desired, press `FREQ BUS`. Then enter a node number between 1 and 7.
5. Press `BUS MEAS on OFF` to activate the bus measurement. The menu changes to `BUS MEAS ON off`. The DC or frequency bus measurement value is displayed in the marker value. See the *Bus Measurement Values* section.
6. Observe the bus measurement trace and marker value.
7. Press (Preset) to exit the bus measurement.

To change the bus node to another node, repeat the steps above.

Both the DC bus and the frequency bus can be monitored simultaneously. This helps when observing the relationship between the VCO tuning voltage and the VCO output frequency of the fractional N oscillator. See the *Bus Measurement Values* section.

Bus Measurement Values

The bus measurement value is displayed with a unit "U."

- The DC bus measurement's "1 U" is equivalent to "1 V." The displayed value in the DC bus measurement does not corresponding to the measured voltage because the voltage detected at the DC bus node is scaled appropriately and measured. The scaling factor depends on each DC node. For example, the scaling factor at the DC bus node 1 of +5 V (AUX) is approximately 0.405. Therefore the displayed value is nominally 2.025 U (5 U x 0.405). A typical value for each DC bus node measurement is provided in the *DC Bus Node Descriptions*.
- The frequency bus measurement's "1 U" is equivalent to "1 MHz." For example, a measured value of 1 kHz is displayed as 1 mU. A typical value for each frequency bus measurement is provided in the *Frequency Bus Node Descriptions*.

The DC bus measurement values are displayed using real format. The frequency bus measurement values are displayed using imaginary format. When a DC or Frequency bus node is measured, the **Re** or **Im** notation appears on the display and indicates the used format. When both a DC bus node and a frequency bus node are measured simultaneously, the DC bus versus frequency bus measurement values are displayed using a polar chart format. This is helpful to observe the relationship between the VCO tuning voltage and the VCO output frequency of the fractional N oscillator.

DC Bus Node Descriptions

The following paragraphs describe the 26 DC bus nodes. They are listed in numerical order.

0: OFF

The DC bus is off. This is the default setting.

1: +5 V (AUX) (2.025 U)

This node is located on the A2 post-regulator and detects the voltage of the +5 V (AUX) power supplied to the A2 post- regulator.

To observe this node, perform the steps in the *Bus Measurement Procedure* . When this node is selected, the trace is typically flat at approximately +2.025 U (±10%).

2: −15 V (−1.92 U)

This node is located on the A2 post-regulator and detects the voltage of the +5 V (AUX) power supplied to the analog boards.

To observe this node, perform the steps in the *Bus Measurement Procedure* . When this node is selected, the trace is typically flat at approximately −1.92 U (±10%).

3: −12.6 V (−2.124 U)

This node is located on the A2 post-regulator and detects the voltage of the −12.6 V power supplied to the probe power connectors on the front panel.

To observe this node, perform the steps in the *Bus Measurement Procedure* . When this node is selected, the trace is typically flat at approximately −2.124 U (±10%).

4: −5 V (−2.025 U)

This node is located on the A2 post-regulator and detects the voltage of the −5 V power supplied to the analog boards.

To observe this node, perform the steps in the *Bus Measurement Procedure* . When this node is selected, the trace is typically flat at approximately −2.025 U (±10%).

5: + 5 V (2.025 U)

This node is located on the A2 post-regulator and detects the voltage of the +5 V power supplied to the analog boards.

To observe this node, perform the steps in the *Bus Measurement Procedure* . When this node is selected, the trace is typically flat at approximately +2.025 U (±10%).

6: + 5.3 V (2.1465 U)

This node is located on the A2 post-regulator and detects the voltage of the +5.3 V power supplied to the A3A3 source.

To observe this node, perform the steps in the *Bus Measurement Procedure* . When this node is selected, the trace is typically flat at approximately +2.1465 U (±10%).

7: + 8.5 V (1.8955 U)

This node is located on the A2 post-regulator and detects the voltage of the +8.5 V power supplied to the A3A3 source.

To observe this node, perform the steps in the *Bus Measurement Procedure* . When this node is selected, the trace is typically flat at approximately +1.8955 U (±10%).

8: + 15 V (AUX) (1.92 U)

This node is located on the A2 post-regulator and detects the voltage of the +15 V (AUX) power supplied to the probe power connectors on the front panel.

To observe this node, perform the steps in the *Bus Measurement Procedure* . When this node is selected, the trace is typically flat at approximately +1.8955 U (±5%).

9: + 15 V (1.92 U)

This node is located on the A2 post-regulator and detects the voltage of the +15 V power supplied to the analog boards.

To observe this node, perform the steps in the *Bus Measurement Procedure* . When this node is selected, the trace is typically flat at approximately +1.92 U (±10%).

10: + 22 V (2.002 U)

This node is located on the A2 post-regulator and detects the voltage of the +22 V power supplied to the S-parameter test set through the TEST SET-I/O INTERCONNECT connector on the rear panel.

To observe this node, perform the steps in the *Bus Measurement Procedure* . When this node is selected, the trace is typically flat at approximately +2.002 U (±10%).

11: FAN POWER

This node is located on the A2 post-regulator and detects the voltage of the FAN POWER (nominal 24 V) supplied to the fan on the rear panel.

To observe this node, perform the steps in the *Bus Measurement Procedure* . The typical trace is shown in Figure 10-7.

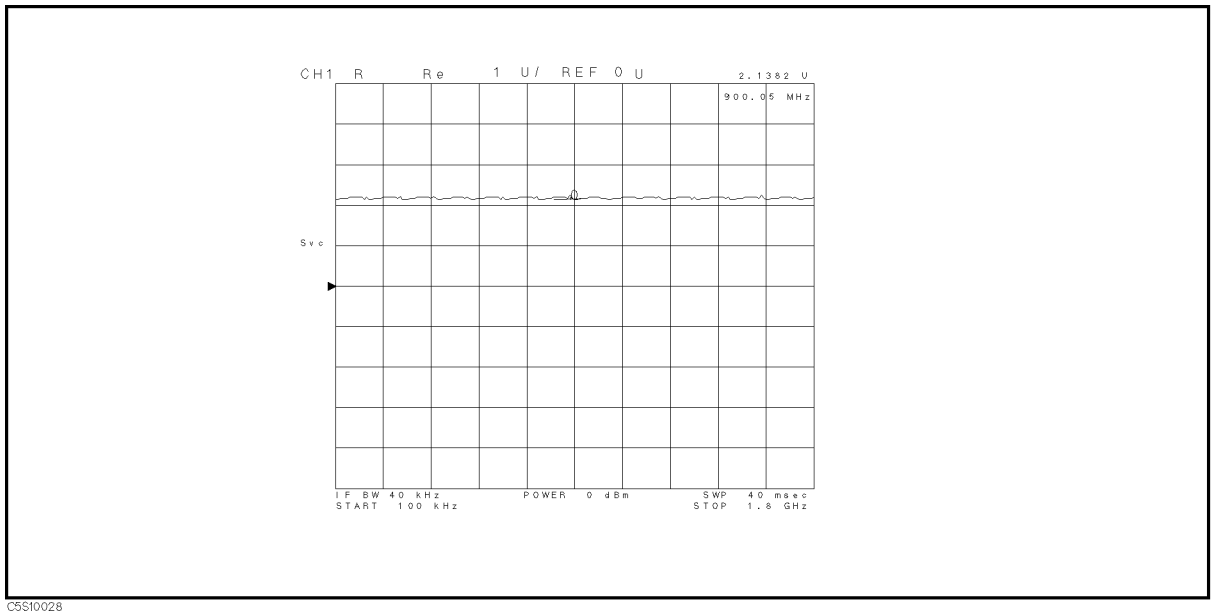


Figure 10-7. Fan Power Typical Trace

12: +65 V (2.0605 U)

This node is not connected to anywhere. Ignore this node.

13: SRC VTUNE (Source Oscillator VCO Tuning Voltage)

This node is located in the source oscillator on the A3A1 Source Vernier and detects the 85.68 MHz VCO tuning voltage.

To observe this node, perform the steps in the *Bus Measurement Procedure* . When this node is selected, the trace is typically flat and within +0.1 U to +3.0 U.

14: 2ND LO VTUNE (Second Local Oscillator VCO Tuning Voltage)

This node is located in the second local oscillator on the A3A2 2nd LO and detects the 1.04 GHz VCO tuning voltage.

To observe this node, perform the steps in the *Bus Measurement Procedure* . When this node is selected, the trace is typically flat and within −130 mU to +130 mU.

15: DET OUT (Detector Output)

This node is located in the level detector circuit on the A3A1 Source Vernier and detects the level detector voltage that loops back from A3A3 source.

16: SRC LO LEVEL

This node is located in the source oscillator circuit on the A3A1 Source Vernier and detects the source VCXO output voltage.

17: DAC OUT (Level DAC Output Voltage)

This node is located in the level vernier circuit on the A3A1 Source Vernier and detects the level DAC output voltage.

18: 1ST LO VTUNE (First Local Oscillator VCO Turning Voltage)

This node is located in the 1st local oscillator on the A4A1 1st LO and detects the 2.05858 GHz to 3.85858 GHz VCO tuning voltage.

The typical trace for the following keystrokes' setting is displayed in Figure 10-8. The displayed trace is typically straight. The typical marker value is within −2.3 U to −1.2 U at a frequency of 1 MHz and within +0.1 U to +1.9 U at a frequency 1.8 GHz.

To observe this trace, perform the steps in the *Bus Measurement Procedure* . At step 2 in the procedure, press the following keys:

(Preset), (Sweep), NUMBER of POINTS, (5), (x1)

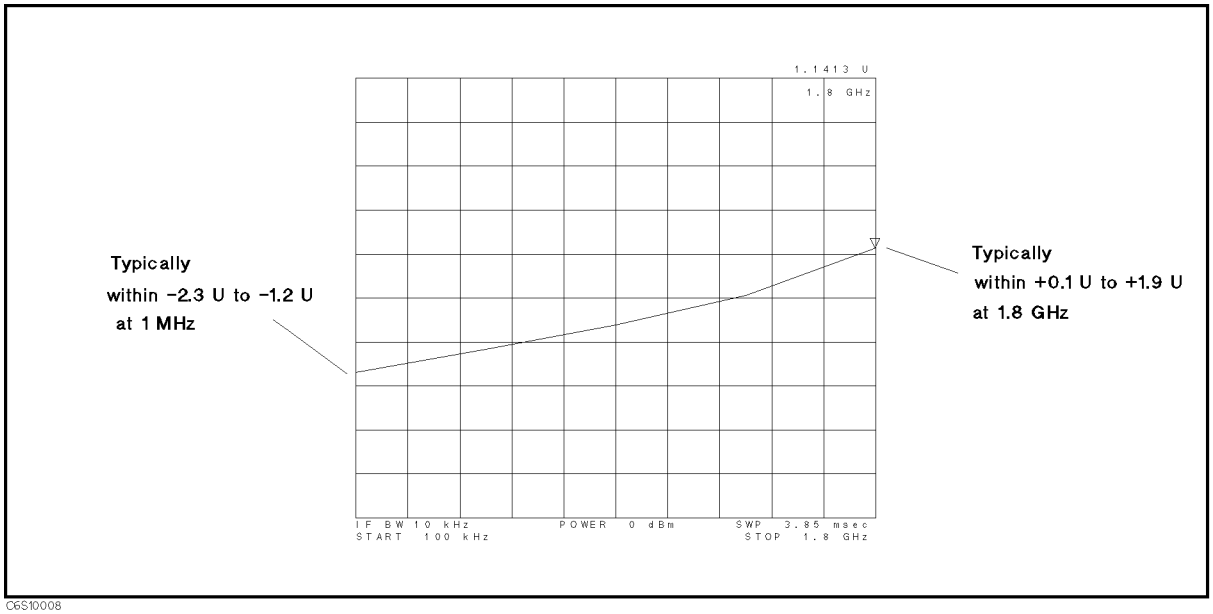


Figure 10-8. 1st LO VTUNE Typical Trace

19: STEP VTUNE (Step Oscillator VCO Turning Voltage)

This node is located in the step oscillator on the A5 synthesizer and detects the 470 MHz to 930 MHz VCO tuning voltage.

The typical trace for the following keystrokes' setting is flat and within 0 U to +2 U. The typical values for the three center frequency ranges are provided in Table 10-2.

To observe this trace, perform the steps in the *Bus Measurement Procedure* . At step 2 in the procedure, press the following keys:

(Preset), (Span), (0), (x1), (Center), (1) (M/μ)

Table 10-2. Typical STEP VTUNE Values

Center Frequency	Typical STEP VTUNE Value
1 MHz Hz to 400 MHz	0 U to +2 U
400 Hz to 1 GHz	0 U to +3 U
1 GHz Hz to 1.8 GHz	+0.5 U to +4 U

20: FN VTUNE (Fractional N Oscillator VCO Turning Voltage)

This node is located in the fractional N oscillator on the A5 synthesizer and detects the 31.25 MHz to 62.5 MHz VCO tuning voltage.

The typical trace for the following keystrokes' setting is displayed in Figure 10-9. The displayed trace is typically flat and higher than −2 U.

To observe this trace, perform the steps in the *Bus Measurement Procedure* . At step 2 in the procedure, press the following keys:

Preset, NUMBER of POINTS, 5, x1

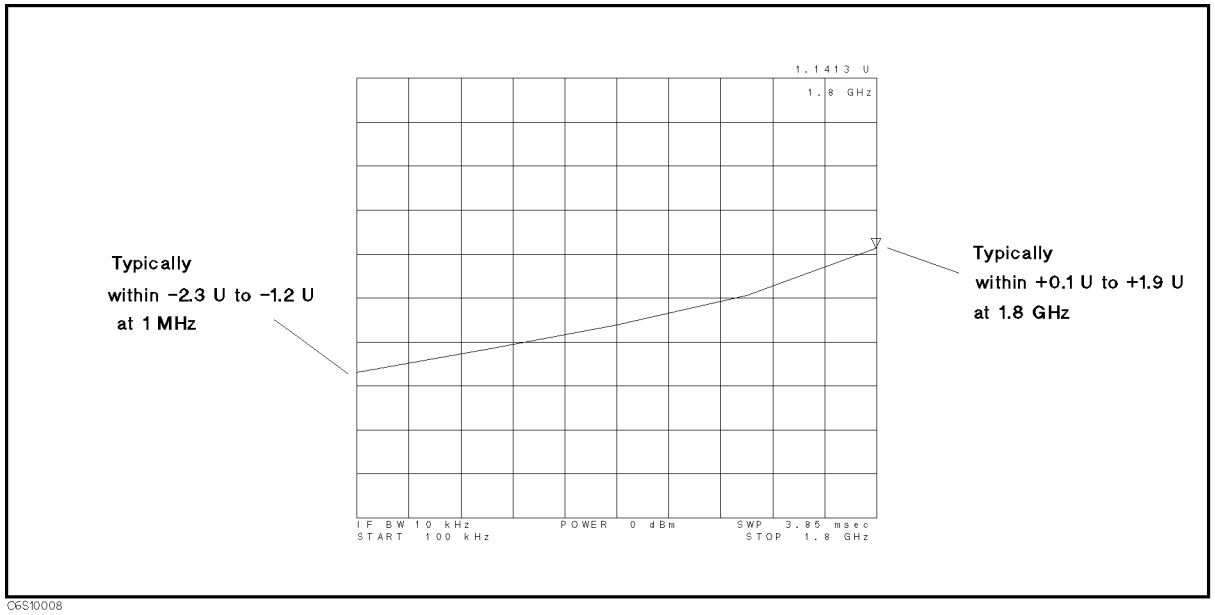


Figure 10-9. FN VTUNE Typical Trace

21: FN INTEG OUT (Fractional N Oscillator Integrator Output Voltage)

This node is located in the fractional N oscillator on the A5 synthesizer and detects the integrator output voltage.

The typical trace for the following keystrokes' setting is displayed in Figure 10-10. The displayed trace is typically straight.

To observe this trace, perform the steps in the *Bus Measurement Procedure* . At step 2 in the procedure, press the following keys:

Preset, Sweep, NUMBER of POINTS, 5, x1,

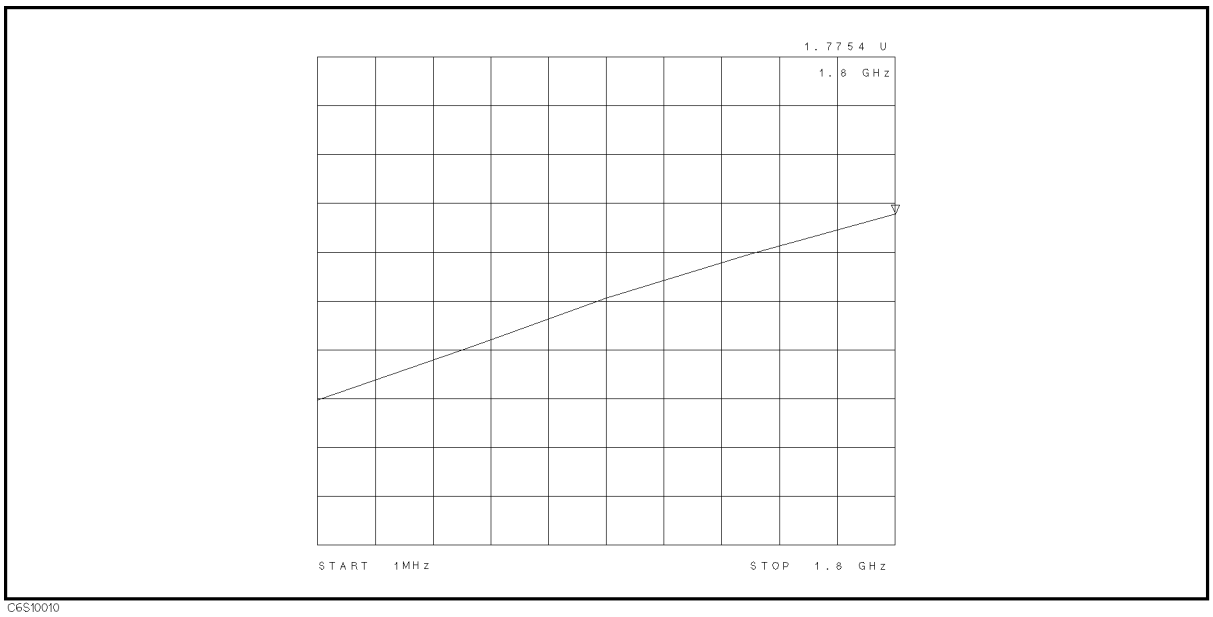


Figure 10-10. FN INTEG OUT Typical Trace

22: REF VTUNE (Reference Oscillator VCO Tuning Voltage)

This node is located in the reference oscillator on the A5 synthesizer and detects the 40 MHz VCXO tuning voltage.

To observe this node, perform the steps in the *Bus Measurement Procedure* . When this node is selected, the trace is typically flat and within 0 U to +3.0 U.

23: 3RD LO VTUNE (Third Local Oscillator VCO Tuning Voltage)

This node is located in the third local oscillator on the A6 receiver IF and detects the 85.6 MHz VCXO tuning voltage.

To observe this node, perform the steps in the *Bus Measurement Procedure* . When this node is selected, the trace is typically flat and within +0.1 U to +3.0 U.

24: 3RD LO LEVEL

This node is located in the A6 receiver IF and detects the third local oscillator signal level. To observe this node, perform the steps in the *Bus Measurement Procedure* .

25: AD VREF (A/D Converter Voltage Reference)

This node is located in the A6 receiver IF and detects the reference voltage of the A/D converter.

The typical trace at preset condition is flat and within +0.16 U to +0.24.

To observe this node, perform the steps in the *Bus Measurement Procedure* .

26: DC BIAS VOLTAGE

This node is located on the A23 DC bias 2/2 and detects the DC bias voltage. To observe this node, perform the steps in the *Bus Measurement Procedure* .

When this node is selected, the trace is typically 1/10 of the DC bias voltage setting.

27: DC BIAS CURRENT

This node is located on the A23 DC bias 2/2 and detects the DC bias current. To observe this node, perform the steps in the *Bus Measurement Procedure* .

When this node is selected, the trace is typically 100/9 [V] of the DC bias current setting [I].

28: GND A22A23

This node is located on the A23 DC bias 2/2 and detects the ground voltage of the DC bias circuit. To observe this node, perform the steps in the *Bus Measurement Procedure* .

When this node is selected, the trace is typically flat and within −0.1 to 0.1 V.

29: GND

This node is located on the A2 post-regulator and detects the ground voltage. To observe this node, perform the steps in the *Bus Measurement Procedure* .

When this node is selected, the trace is typically flat and within −0.1 to 0.1 V.

Frequency Bus Node Descriptions

The following paragraphs describe the 6 frequency bus nodes. They are listed in numerical order.

0: OFF

The frequency bus is off. This is the default setting.

1: SOURCE OSC (Source Oscillator)

This node is located in the source oscillator on the A3A1 Source Vernier and measures the loop back frequency of 40 kHz from the 85.68 MHz VCO.

The typical trace is flat and within +39.992 mU to +40.008 mU.

To observe this node, perform the steps in the *Bus Measurement Procedure* . At step 2 in the procedure, press the following keys:

Preset, Sweep, NUMBER OF POINTS, 2, x1

2: DIVIDER OUT (Divider Output)

This node is located in the divider on the A3A1 Source Vernier and measures the 1/200 divider output frequency 40 kHz.

The typical trace is flat and within +39.992 mU to +40.008 mU.

To observe this node, perform the steps in the *Bus Measurement Procedure* . At step 2 in the procedure, press the following keys:

Preset, Sweep, NUMBER OF POINTS, 1, 0, x1

3: STEP OSC (Step Oscillator)

This node is located in the step oscillator on the A5 synthesizer and measures the step oscillator frequency through the 1/256 divider.

The typical trace is flat and the trace value depends on the measurement settings (center and span settings). The typical values for several settings are provided in Table 7-1 STEP OSC Frequency in chapter 7.

4: FN OSC (Fractional N Oscillator)

This node is located in the fractional N oscillator on the A5 synthesizer and measures the fractional N oscillator frequency through the 1/16 divider.

The typical trace is flat and the trace value depends on the measurement settings (center and span settings). The typical values for several settings are provided in the *Check the FRAC N OSC Signal* in chapter 7.

5: REF OSC (Reference Oscillator)

This node is located in the INT REF output circuit on the A5 synthesizer and measures the INT REF output frequency 10 MHz through the 1/4 divider.

The typical trace is flat and within +2.4996 U to +2.5004 U.

To observe this node, perform the steps in the *Bus Measurement Procedure* . At step 2 in the procedure, press the following keys to make a fast sweep.

(Preset), (Sweep), NUMBER OF POINTS, (1), (0), (x1)

6: 3RD LO OSC (Third Local Oscillator)

This node is located in the third local oscillator on the A6 receiver IF and measures the loop back frequency of 40 kHz from the 85.6 MHz/85.68 MHz VCO.

The typical trace is flat and within +39.992 mU to +40.008 mU.

To observe this node, perform the steps in the *Bus Measurement Procedure* . At step 2 in the procedure, press the following keys to make a fast sweep.

(Preset), (Sweep), NUMBER OF POINTS, (1), (0), (x1)

7: SAMPLE HOLD

This node is located in the sequencer on the A6 receiver IF and measures the 80 kHz sampling signal in the sequencer.

The typical trace is flat and within +79.984 mU to +80.016 mU.

To observe this node, perform the steps in the *Bus Measurement Procedure* . At step 2 in the procedure, press the following keys to make a fast sweep.

(Preset), (Sweep), NUMBER OF POINTS, (1), (0), (x1)

CORRECTION CONSTANTS MENU

Figure 10-11 shows the correction constants menu. This menu allows you to turn off one (or more) of the corrections. When one (or more) corrections are turned off, the analyzer displays the raw measured data. You can check the raw characteristics of the source and receiver circuit. For the corrections, see the *Correction Constants*.

To display the menu, press System, SERVICE MENU, SERVICE MODES, and CORRECTION CONSTANTS. Each softkey in the correction constants menu is described below.

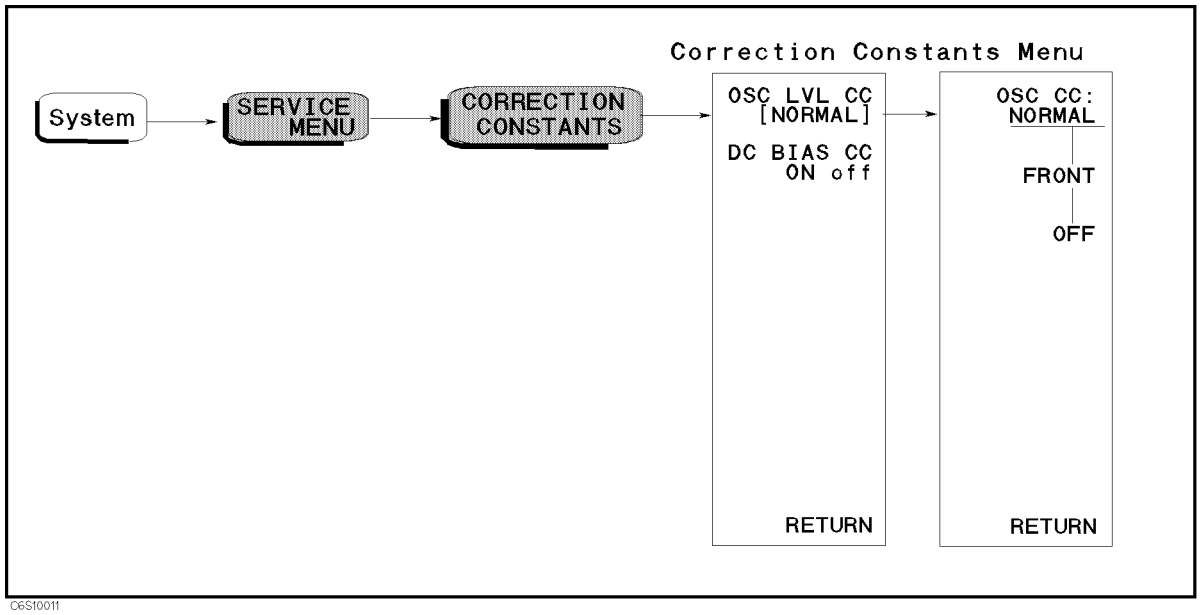


Figure 10-11. Correction Constants Menu

OSC LVL CC [ ] (:DIAG:SERV:CCON:OLEV {NORM|FRON|OFF})

Displays the control menu that allows you to select one of the OSC level correction constants settings of normal, front panel, and off. The softkeys in this control menu are described below. The abbreviation of the current setting is displayed in the brackets of the menu.

OSC CC: NORMAL	sets the OSC level correction constants to normal mode. In this mode, the OSC level setting applies to the measurement terminal.
FRONT	sets the OSC level correction constants to front panel mode. In this mode, the OSC level setting applies to the mainframe front "S" output.
OFF	sets the OSC level correction constants to off. In this mode, the OSC level is not corrected.

`DC BIAS CC ON/off` (`:DIAG:SERV:CCON:DCB {OFF|ON|0|1}`)

Toggles the DC bias level correction on and off. When this correction is turned off, the analyzer does not perform the compensation using the DC bias level correction constants.

Note All corrections must be turned to on except when checking the analog circuits.

Correction Constants

The analyzer has the following two correction constants in the EEPROM on the A1 CPU. It uses them to control the internal circuits and to achieve optimum performance by compensating for errors due to circuit characteristics. Each of the correction constants is described below. For the circuits that appear in the following description, see Chapter 11.

- **OSC Level Correction Constants** are control values for the level DAC in the A3A1 Source Vernier. These affect the following performance specifications:

  OSC Level Accuracy.

- **DC Bias Correction Constants** are control values for the level DACs in the A22 DC bias 1/2. These affect the following performance specifications:

  DC Bias Level Accuracy

SYNTHESIZER CONTROL MENU

Figure 10-12 shows the synthesizer control menus. To display the synthesizer control menu, press System, SERVICE MENU, SERVICE MODES, and SYNTH. Each softkey in the synthesizer control menu is described below.

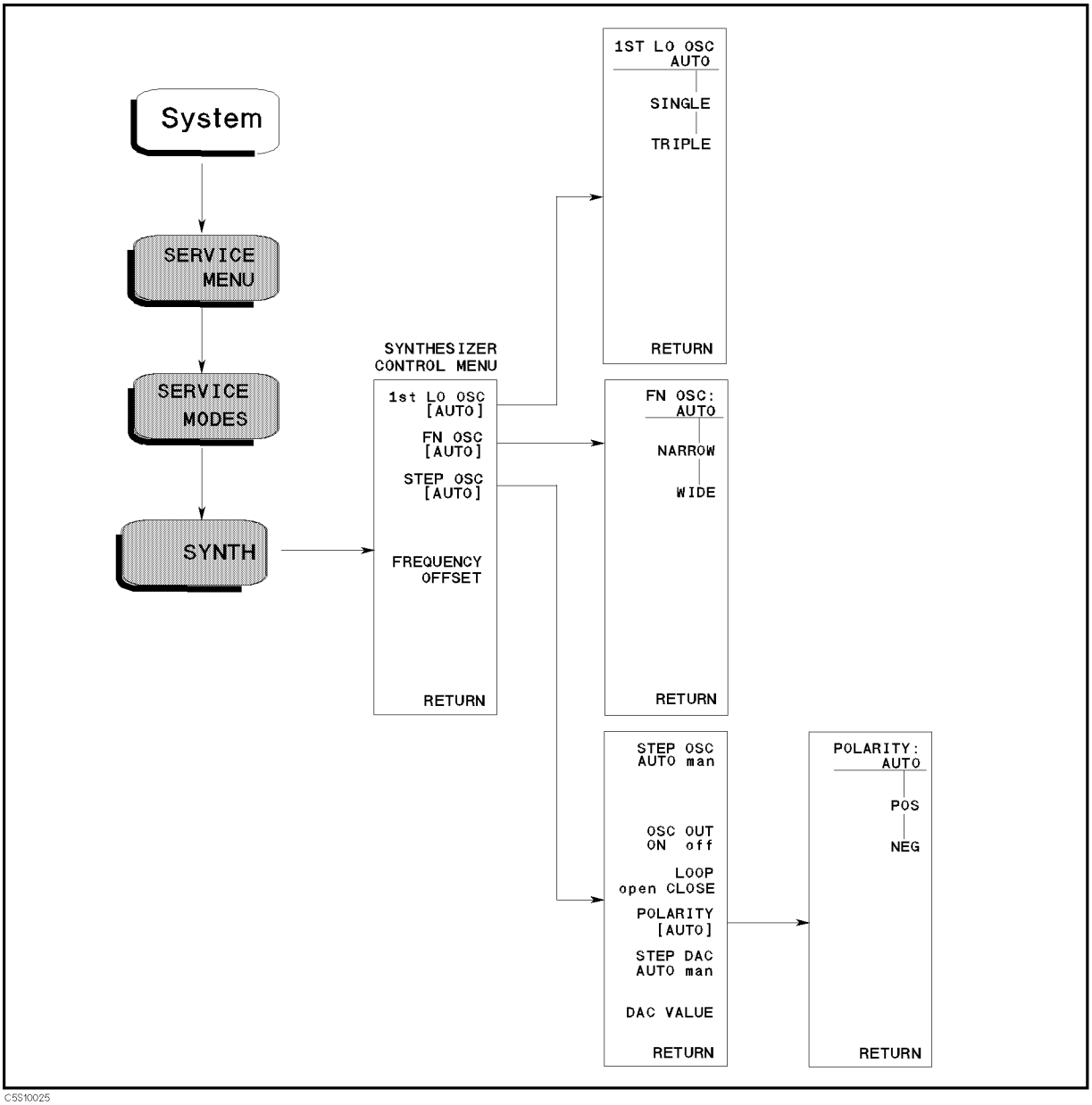


Figure 10-12. Synthesizer Control Menu

1st LO OSC [ ] (:DIAG:SYNT:FLOC:MODE {AUTO|SING|TRIP})

Displays the control menu that allows you to control the 1st LO (first local oscillator) in the A4A1 1st LO. The softkeys in this control menu are described below. The abbreviation of the current setting (auto, single, or triple) is displayed in the brackets of the menu.

1ST LO OSC: AUTO	sets the 1st LO control to the automatic mode (normal operation). In this mode, the analyzer controls the 1st LO automatically according to the measurement settings.
SINGLE	sets the 1st LO to single mode.
TRIPLE	sets the 1st LO to triple mode.

FN OSC [ ] (:DIAG:SERV:STNT:FN:MODE {AUTO|NARR|WIDE})

Displays the control menu that allows you to control the FN OSC (fractional N oscillator) in the A5 synthesizer. The softkeys in this control menu are described below. The abbreviation of the current setting (auto, narrow, or wide) is displayed in the brackets of the menu.

FN OSC: AUTO	sets the FN OSC control to automatic mode (normal operation). In this mode, the analyzer set the FN OSC setting to the narrow, or wide automatically according to the measurement setting.
NARROW	sets the FN OSC to narrow mode.
WIDE	sets the FN OSC to wide mode.

STEP OSC [ ]

Displays the control menus that allow you to control the STEP OSC (step oscillator) in the A5 synthesizer. The softkeys in these control menus are described below. The abbreviation of the current setting (AUTO or MANUAL) is displayed in the brackets of the menu.

STEP OSC AUTO man (:DIAG:SERV:SYNT:STEP:MODE {AUTO|MAN})

Toggles the STEP OSC control mode to automatic mode (normal operation) or manual mode. In the automatic mode, the analyzer controls the STEP OSC automatically according to the measurement setting. In the manual mode, the STEP OSC is controlled by the following softkeys.

OSC OUT ON off (:DIAG:SERV:SYNT:STEP:OUTP {OFF|ON|0|1})

Toggles the STEP OSC output to on or off.

LOOP open CLOSE (:DIAG:SERV:SYNT:STEP:LOOP {OPEN|CLOSE})

Toggles the phase locked loop of the STEP OSC to open or close.

`POLARITY [ ]` (:DIAG:SERV:SYNT:STEP:POL {AUTO|POS|NEG})

Displays the control menu for ±1 converter in the STEP OSC. The softkeys in this control menu are described below. The abbreviation of the current setting (AUTO, POS, or NEG) is displayed in the brackets of the menu.

`POLARITY: AUTO` sets the ±1 converter control to automatic mode. In this mode, the analyzer selects one of the ±1 converter automatically according to the measurement setting.

`POS` selects the +1 converter.

`NEG` selects the −1 converter.

`STEP DAC AUTO man` (:DIAG:SERV:SYNT:STEP:DAC:MODE {AUTO|MAN})

Toggles the STEP DAC mode in the STEP LO to automatic mode or manual mode. In the automatic mode, the analyzer sets the STEP DAC control value according to the measurement settings. In the manual mode, the STEP DAC control value is set by using the `DAC VALUE` softkey.

`DAC VALUE` (:DIAG:SERV:SYNT:STEP:DAC:VAL <*numeric*>)

Allows you to enter the STEP DAC control value (0 to 4095). This value is used when the STEP DAC is set to manual mode.

`FREQUENCY OFFSET` (:DIAG:SERV:SYNT:FREQ:OFFS

<*numeric*>)

Allows you to enter the frequency offset value. Factory use only.

Note All settings must be turned to auto except when checking the analog circuits.

OSC CONTROL MENU

Figure 10-13 shows the OSC control menu hierarchy. To display the OSC control menu, press System, SERVICE MENU, SERVICE MODES, and OSC. Each softkey in the OSC control menus is described below.

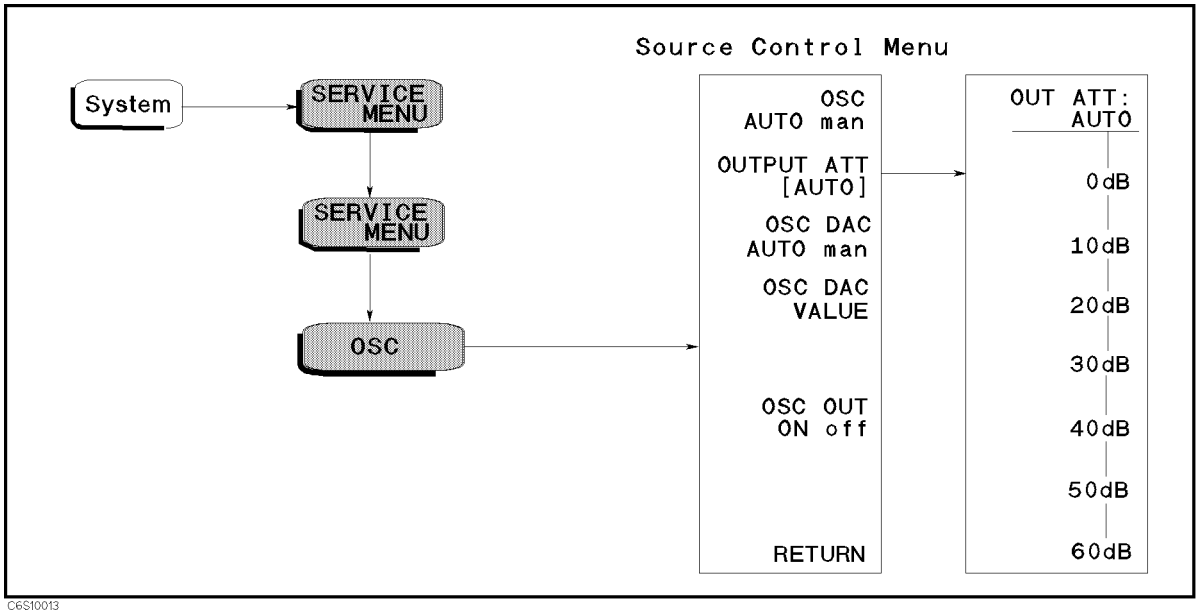


Figure 10-13. OSC Control Menu

OSC AUTO man (:DIAG:SERV:SOUR:MODE {AUTO|MAN})

Toggles the OSC control mode to automatic mode and manual mode. In the automatic mode, the analyzer sets the OSC level automatically according to the measurement settings. In the manual mode, the OSC level is controlled by the following softkeys.

OUTPUT ATT [ ] (:DIAG:SERV:SOUR:ATT {AUTO|DB0|DB10|DB20|DB30|DB40|DB50|DB60})

Displays the control menu that allows you to control the A7 output attenuator. The softkeys in this control menu are described below. The abbreviation of the current setting is displayed in the brackets of the menu.

`OUT ATT: AUTO` sets the A7 control to automatic mode. In this mode, the analyzer controls the A7 automatically according to the measurement setting.

`0 dB` sets the A7 output attenuator to 0 dB.

`10 dB` sets the A7 output attenuator to 10 dB.

`20 dB` sets the A7 output attenuator to 20 dB.

`30 dB` sets the A7 output attenuator to 30 dB.

`40 dB` sets the A7 output attenuator to 40 dB.

`50 dB` sets the A7 output attenuator to 50 dB.

`60 dB` sets the A7 output attenuator to 60 dB.

`OSC DAC AUTO man` (:DIAG:SERV:SOUR:LEV:DAC:MODE {AUTO|MAN})

Toggles the OSC DAC control mode in the A3A1 source vernier to automatic mode and manual mode. In the automatic mode, the analyzer sets the OSC DAC according the measurement settings. In the manual mode, the OSC DAC output is controlled by the `OSC DAC VALUE` softkey.

`OSC DAC VALUE` (:DIAG:SERV:SOUR:LEV:DAC:VAL <*numeric*>)

Allows you to enter the level DAC control value (0 to 32767). This value is used when the OSC DAC control mode is set to manual.

`OSC OUT ON off` (:DIAG:SERV:SOUR:STAT {OFF|ON|0|1})

Toggles the OSC switch in the A3A1 source vernier to turn on and off the OSC signal.

Note All settings must be turned to auto except when checking the analog circuits.

DC BIAS CONTROL MENU

Figure 10-14 shows the DC bias control menu hierarchy. To display the DC bias control menu, press System, SERVICE MENU, SERVICE MODES, and DC BIAS. Each softkey in the source control menus is described below.

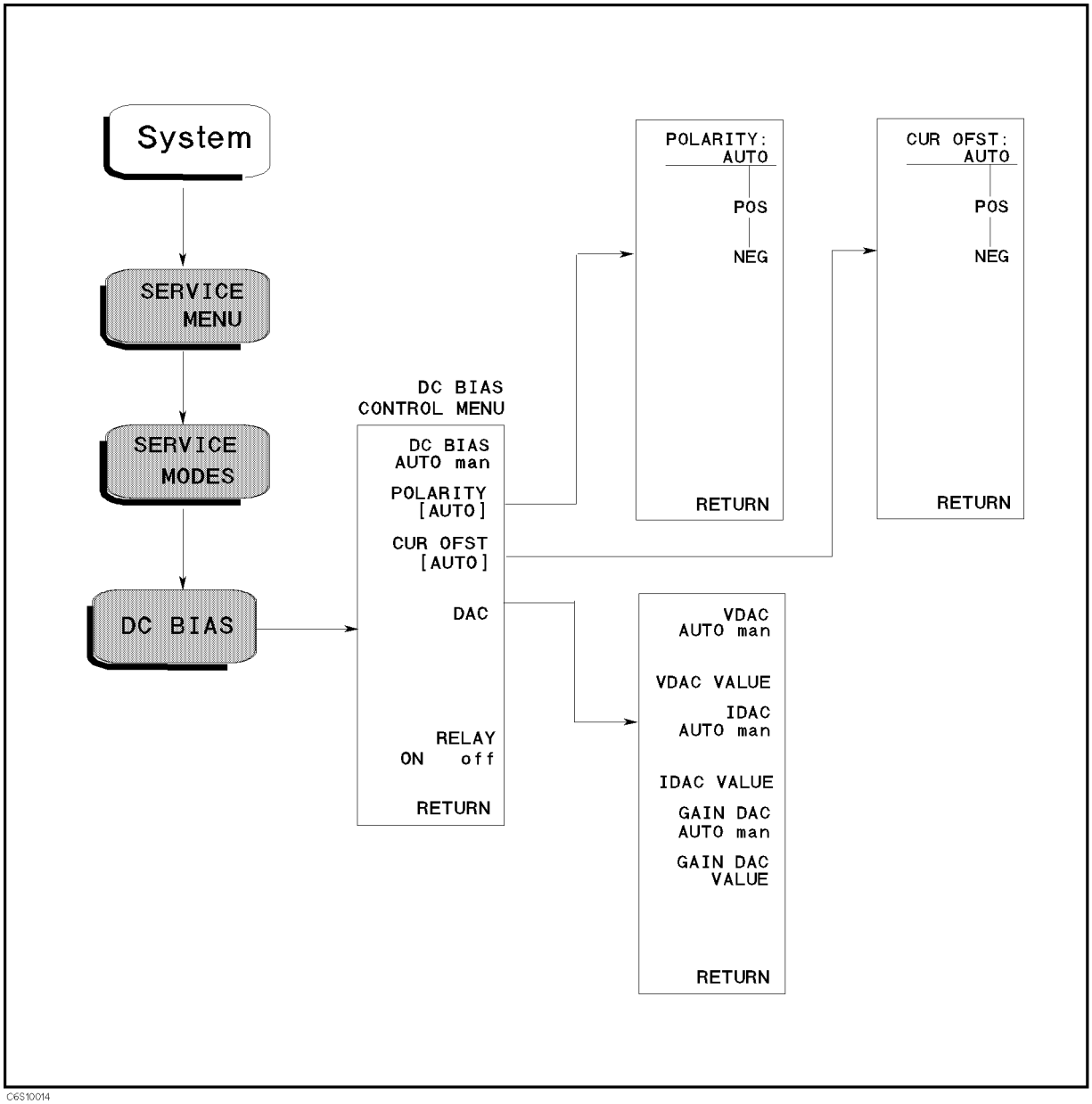


Figure 10-14. DC Bias Control Menu

DC BIAS AUTO man (:DIAG:SERV:DCB:MODE {AUTO|MAN})

Toggles the DC bias control mode to automatic mode and manual mode. In the automatic mode, the analyzer sets the DC bias automatically according to the measurement settings. In the manual mode, the DC bias is controlled by the following softkeys.

POLARITY [ ] (:DIAG:SERV:DCB:POL {AUTO|POS|NEG})

Displays the control menu that allows you to control the DC bias polarity control in A22 DC bias 1/2. The softkeys in this control menu are described below. The abbreviation of the current setting is displayed in the brackets of the menu.

POLARITY: AUTO sets the DC bias polarity control to automatic mode. In this mode, the analyzer controls the A22 automatically according to the measurement setting.

POS sets the DC bias polarity control to positive.

NEG sets the DC bias polarity control to negative.

CUR OFST [ ] (:DIAG:SERV:DCB:OFFS {AUTO|POS|NEG})

Displays the control menu that allows you to control the DC bias current offset. The softkeys in this control menu are described below. The abbreviation of the current setting is displayed in the brackets of the menu.

CUR OFST: AUTO sets the DC bias current offset to automatic mode. In this mode, the analyzer set the current offset automatically according to the measurement setting.

POS sets the DC bias current offset to positive.

NEG sets the DC bias current offset to negative.

DAC

Displays the control menus that allow you to control the DC bias level DACs in the A22 DC bias 1/2. The softkeys in the control menu are described below.

VDAC AUTO man (:DIAG:SERV:DCB:VDAC:MODE {AUTO|MAN})

Toggles the VDAC mode in A22 to automatic mode or manual mode. In the automatic mode, the analyzer sets the VDAC control value according to the measurement settings. In the manual mode, the VDAC control value is set by using the VDAC VALUE softkey.

VDAC VALUE (:DIAG:SERV:DCB:VDAC:VAL <*numeric*>)

Allows you to enter the VDAC control value (0 to 65535). This value is used when the VDAC is set to manual mode.

IDAC AUTO man (:DIAG:SERV:DCB:IDAC:MODE {AUTO|MAN})

Toggles the IDAC mode in A22 to automatic mode or manual mode. In the automatic mode, the analyzer sets the IDAC control value according to the measurement settings. In the manual mode, the IDAC control value is set by using the IDAC VALUE softkey.

`IDAC VALUE` (`:DIAG:SERV:DCB:IDAC:VAL` <*numeric*>)

Allows you to enter the IDAC control value (0 to 65535). This value is used when the IDAC is set to manual mode.

`GDAC AUTO man` (`:DIAG:SERV:DCB:GDAC:MODE {AUTO|MAN}`)

Toggles the GAINDAC mode in A22 to automatic mode or manual mode. In the automatic mode, the analyzer sets the GAINDAC control value according to the measurement settings. In the manual mode, the GAINDAC control value is set by using the `GDAC VALUE` softkey.

`GDAC VALUE` (`:DIAG:SERV:DCB:GDAC:VAL` <*numeric*>)

Allows you to enter the GAINDAC control value (0 to 255). This value is used when the GAINDAC is set to manual mode.

`RELAY ON off` (`:DIAG:SERV:DCB:STAT {OFF|ON|0|1}`)

Toggles the DC bias output relay in the A23 DC bias 2/2 to turn on and off the DC bias.

Note All settings must be turned to auto except when checking the analog circuits.

TRANSDUCER CONTROL MENU

Figure 10-15 shows the transducer (TRD) control menu hierarchy. To display the TRD control menu, press System, SERVICE MENU, SERVICE MODES, and TRD. A softkey in the TRD control menu displays one of menus used to control one of the A41 TRD amp circuits. Each softkey in the TRD control menu is described below.

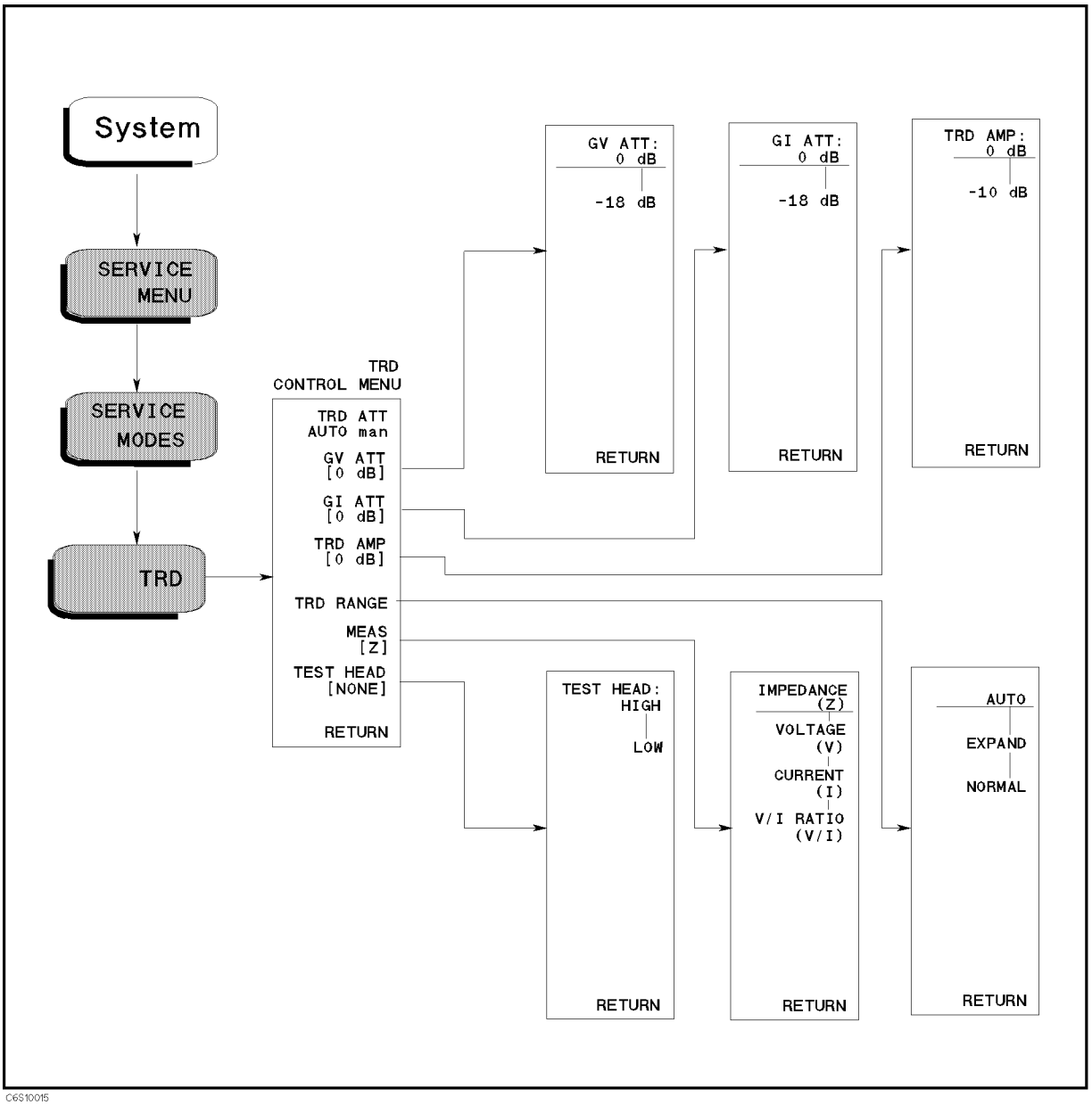


Figure 10-15. TRD Control Menu

TRD ATT AUTO man (:DIAG:SERV:TRAN:MODE {AUTO|MAN})

Toggles the TRD gain control mode to automatic mode (normal operation) or manual mode. In the automatic mode, the analyzer controls the TRD gains GV ATT, GI ATT, and TRD AMP settings automatically according to the measurement setting. In the manual mode, the TRD gains are controlled by the following softkeys.

GV ATT [ ] (:DIAG:SERV:TRAN:GVAT {DB0|DB18})

Displays the control menu for the GV ATT. The softkeys in this control menu are described below. The abbreviation of the current setting (, 0 dB, or −18 dB) is displayed in the brackets of the menu.

GV ATT: 0dB — sets the TRD GV ATT setting to 0 dB.

−18 dB — sets the TRD GV ATT setting to −18 dB.

GI ATT [ ] (:DIAG:SERV:TRAN:GIAT {DB0|DB18})

Displays the control menu for the GI ATT. The softkeys in this control menu are described below. The abbreviation of the current setting (, 0 dB, or −18 dB) is displayed in the brackets of the menu.

GI ATT: 0dB — sets the TRD GI ATT setting to 0 dB.

−18 dB — sets the TRD GI ATT setting to −18 dB.

TRD AMP [ ] (:DIAG:SERV:TRAN:GAIN {DB0|DB10})

Displays the control menu for the TRD AMP. The softkeys in this control menu are described below. The abbreviation of the current setting (, 0 dB, or −10 dB) is displayed in the brackets of the menu.

TRD AMP: 0dB — sets the TRD AMP setting to 0 dB.

−10 dB — sets the TRD AMP setting to −10 dB.

TRD RANGE (:DIAG:SERV:TRAN:RANG {AUTO|EXP|NORM})

Displays the control menu that allows you to control the TRD ranges of auto, expand, and normal. The softkeys in this control menu are described below.

AUTO — sets the TRD range to automatic mode (normal operation). In this mode, the analyzer controls the TRD range setting automatically according to the measurement setting.

EXPAND — sets the TRD range to expand.

NORMAL — sets the TRD range to normal.

MEAS [ ] (:DIAG:SERV:TRAN:SENS:FUNC {IMP|VOLT|CURR|VIR})

Displays the control menu that allows you to select the display parameter from impedance, voltage, current, or voltage divided by current. The softkeys in this control menu are described below. The abbreviation of the current setting is displayed in the brackets of the menu.

IMPEDANCE (Z)	sets the display parameter to impedance.
VOLTAGE (V)	sets the display parameter to voltage.
CURRENT (I)	sets the display parameter to current.
V/I RATIO (V/I)	sets the display parameter to voltage divided by current.

TEST HEAD [ ] (:DIAG:SERV:TRAN:THE {HIMP|LIMP|HTHI|HTLI})

Displays the control menu that allows you to set the analyzer operation of the high impedance, low impedance, high temperature high impedance, and high temperature low impedance test heads. The softkeys in this control menu are described below. The abbreviation of the current setting is displayed in the brackets of the menu.

TEST HEAD: HIGH	sets the analyzer for high impedance test head operation.
LOW	sets the analyzer for low impedance test head operation.
HI TEMP HIGH	sets the analyzer for high temperature high impedance test head operation.
HI TEMP LOW	sets the analyzer for high temperature low impedance test head operation.

Note All settings must be turned to auto except when checking the analog circuits.

IF CONTROL MENU

Figure 10-16 shows the IF control menu hierarchy. To display the IF control menu, press System, SERVICE MENU, SERVICE MODES, and IF. A softkey in the IF control menu displays one of menus used to control one of the A6 receiver IF circuits. Each softkey in the IF control menu is described below.

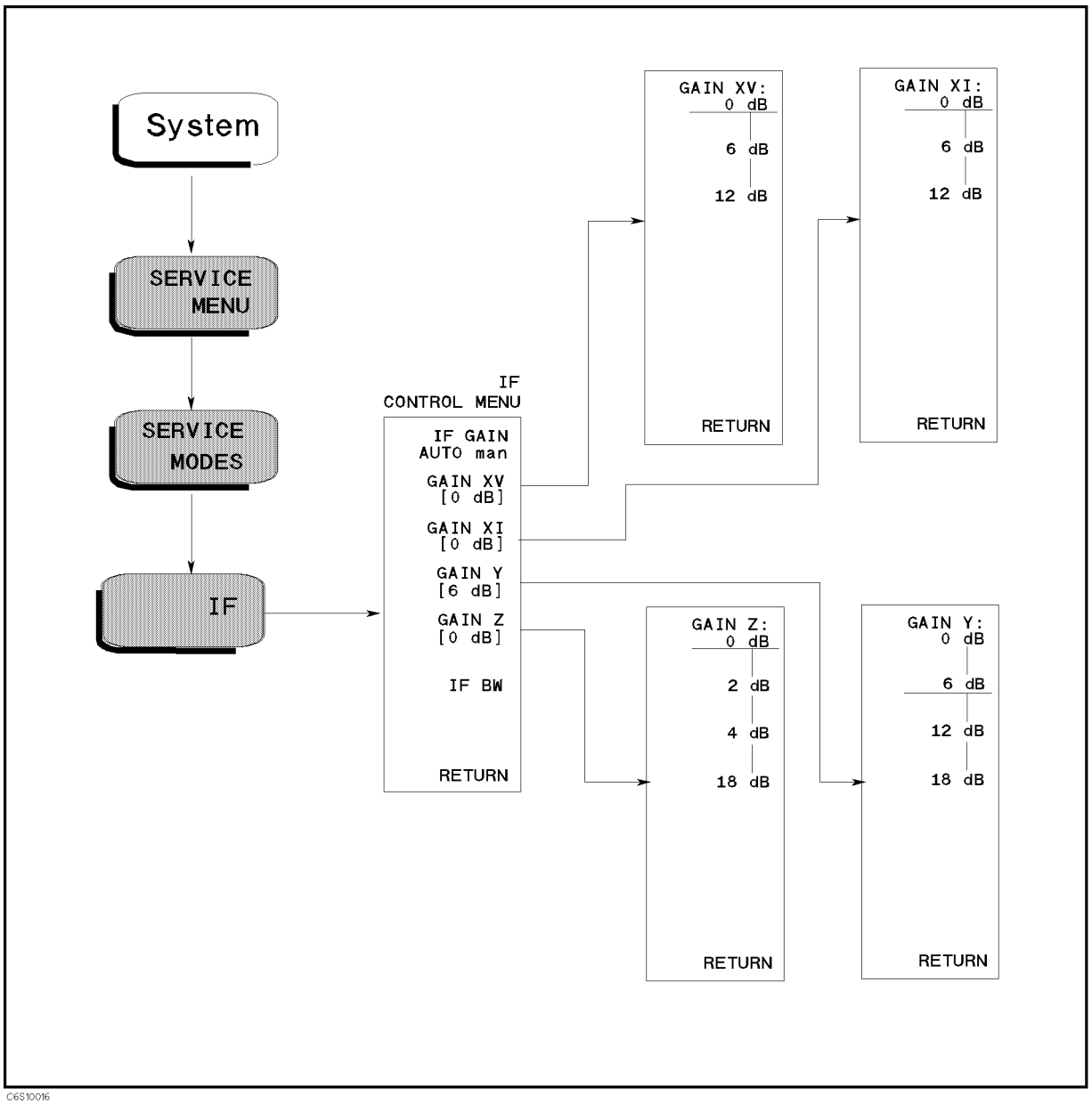


Figure 10-16. IF Control Menu

IF GAIN AUTO man (:DIAG:SERV:IF:GAIN:MODE {AUTO|MAN})

Toggles the IF gain control mode to automatic mode (normal operation) or manual mode. In the automatic mode, the analyzer controls the IF gain XV, XI, Y, and Z settings automatically according to the measurement setting. In the manual mode, the IF gains are controlled by the following softkeys.

GAIN XV [ ] (:DIAG:SERV:IF:GAIN:X:XV {DB0|DB6|DB12})

Displays the control menu for the IF GAIN XV (IF gain X in voltage measurement.) The softkeys in this control menu are described below. The abbreviation of the current setting (0 dB, 6dB, or 12 dB) is displayed in the brackets of the menu.

GAIN XV: 0dB	sets the IF GAIN XV to 0 dB.
6 dB	sets the IF GAIN XV to 6 dB.
12 dB	sets the IF GAIN XV to 12 dB.

GAIN XI [ ] (:DIAG:SERV:IF:GAIN:X:XI {DB0|DB6|DB12})

Displays the control menu for the IF GAIN XI (IF gain X in current measurement.) The softkeys in this control menu are described below. The abbreviation of the current setting (0 dB, 6dB, or 12 dB) is displayed in the brackets of the menu.

GAIN XI: 0dB	sets the IF GAIN XI to 0 dB.
6 dB	sets the IF GAIN XI to 6 dB.
12 dB	sets the IF GAIN XI to 12 dB.

GAIN Y [ ] (:DIAG:SERV:IF:GAIN:Y {DB0|DB6|DB12|DB18})

Displays the control menu for the IF GAIN Y. The softkeys in this control menu are described below. The abbreviation of the current setting (0 dB, 6dB, 12 dB, or 18 dB) is displayed in the brackets of the menu.

GAIN Y: 0dB	sets the IF GAIN Y to 0 dB.
6 dB	sets the IF GAIN Y to 6 dB.
12 dB	sets the IF GAIN Y to 12 dB.
18 dB	sets the IF GAIN Y to 18 dB.

GAIN Z [ ] (:DIAG:SERV:IF:GAIN:Z {DB0|DB2|DB4|DB18})

Displays the control menu for the IF GAIN Z. The softkeys in this control menu are described below. The abbreviation of the current setting (0 dB, 2dB, 4 dB, or 18 dB) is displayed in the brackets of the menu.

GAIN Z: 0dB	sets the IF GAIN Y to 0 dB.
2 dB	sets the IF GAIN Y to 2 dB.
4 dB	sets the IF GAIN Y to 4 dB.
18 dB	sets the IF GAIN Y to 18 dB.

IF BW

Displays the IF band pass filter band width of 1 kHz.

Note All settings must be turned to auto except when checking the analog circuits.

BOOTLOADER MENU

Figure 10-17 shows the Bootloader menus and the associated menus. To display the menu, turn the analyzer on while pressing (Preset). The Bootloader menu is used to install the firmware into the analyzer using a firmware diskette and the built-in FDD. Also these menus are used to make a system backup diskette. Each softkey in the Bootloader menus is described below.

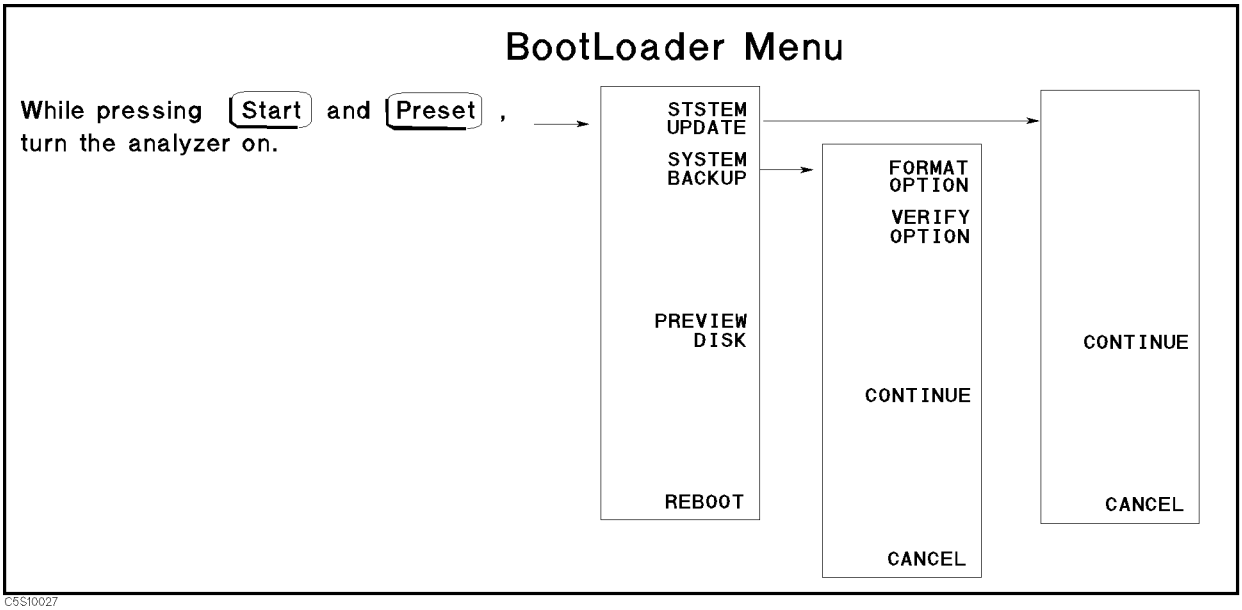


Figure 10-17. Bootloader Menu

SYSTEM UPDATE

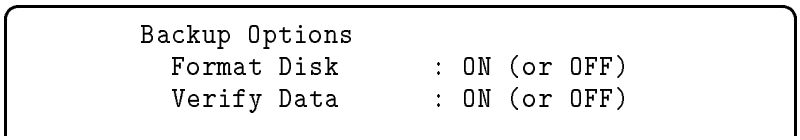
Allows you to install and update the firmware in the analyzer. Before pressing this softkey, insert the firmware diskette into the FDD on the front panel. Then press this softkey to install the firmware from the diskette to the analyzer. The detailed procedure is provided in the *Firmware Installation* in chapter 14.

After pressing this softkey, CONTINUE and CANCEL softkeys appear on the display. Press CONTINUE to continue the firmware installation. Press CANCEL to cancel the firmware installation.

SYSTEM BACKUP

Displays the control menu that allows you to make a system backup diskette in which the current firmware is stored. The applicable diskette is a 3.5 inch 1.44 MByte flexible disk. The softkeys in the control menu are described below.

FORMAT OPTION — toggles format option on and off. When the format option is set to on, the flexible diskette is initialized before storing the firmware. When the format option is set to off, the diskette is not initialized. The default setting is on. The format option setting is displayed as shown below.



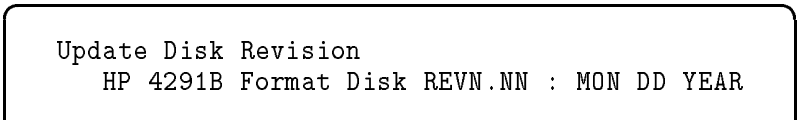
`VERIFY OPTION` toggles verify option on and off. When the verify option is set to on, the system stored in the flexible diskette is verified to be the same as the current firmware in the analyzer after storing the firmware. When the verify option is set to off, the verification is not performed. The default setting is on. The verify option setting is displayed as shown above.

`CONTINUE` continues making the system backup. Before pressing this softkey, insert a diskette into the FDD on the front panel.

`CANCEL` stops making the system backup and return to the Bootloader menu.

PREVIEW DISK

Displays the revision information of the firmware stored in the firmware diskette as shown below. Before pressing this softkey, insert a firmware diskette into the FDD on the front panel.



where N.NN: Revision Number
MON DD YEAR: Implementation Date (Month Day Year)

REBOOT

Reboots the analyzer. If the new firmware is installed, the analyzer boots up using the new firmware. After pressing the softkey, the analyzer performs the normal power on sequence.

11

Theory of Operation

This chapter contains the theory of operation for the analyzer.. It begins with an overall description of the operation of the HP 4291B RF Impedance/Material Analyzer. Then the analyzer 's functional groups are briefly described..

Next, the operation of each group is described to the extent necessary to support assembly level repair. Simplified block diagrams of each group support the group description. Detailed component-level circuit theory is not provided in this manual. Figure 11-10 and Figure 11-11 at the end of the chapter provide additional block diagrams to help you understand the analyzer's operation.

OVERALL ANALYZER OPERATION

The HP 4291B consists of a mainframe, a test station, test heads, and a calibration kit (see Figure 11-1). The mainframe includes a source, a receiver, a digital control, and a power supply.

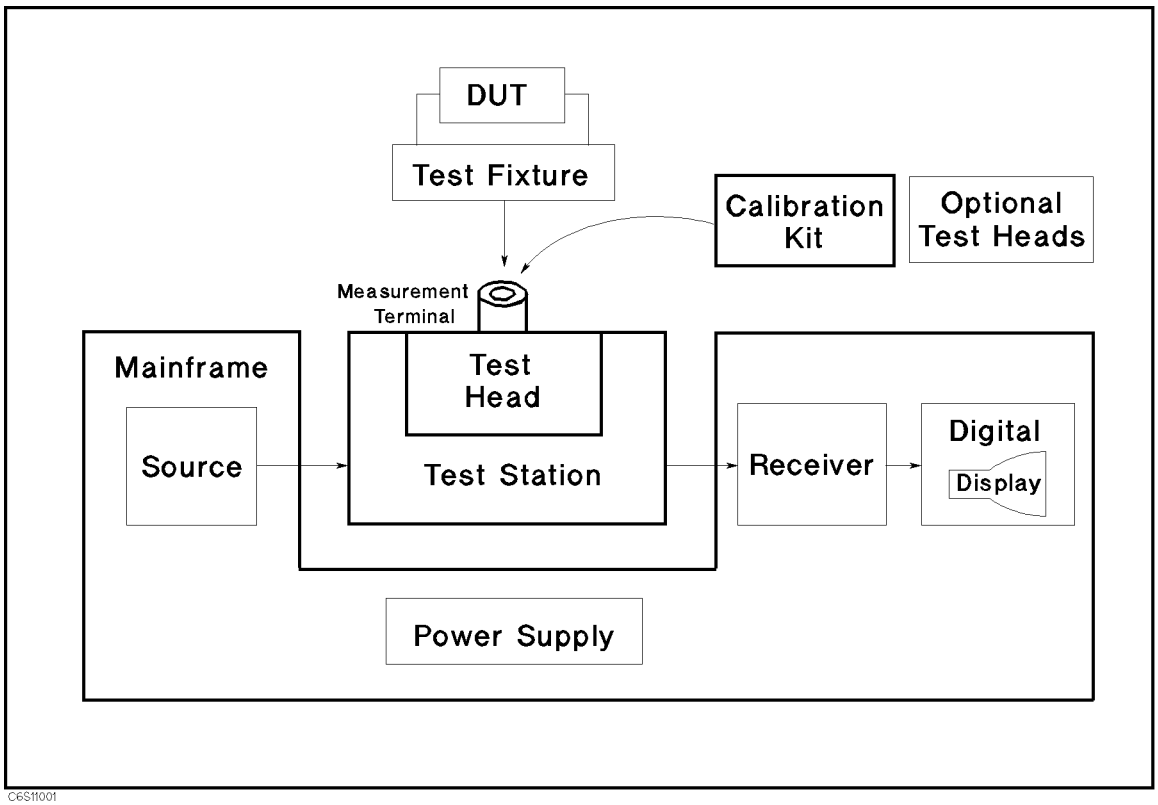


Figure 11-1. Analyzer Simplified Block Diagram

The source generates a stimulus signal in the range of 1 MHz to 1.8 GHz.

The stimulus signal goes through the test station, the test head, and the test fixture to the device under test (DUT).

The test station senses the voltage across the DUT and the current through the DUT. The test station multiplexes the two signals and applies each signal to the receiver.

The receiver converts the signal to a digital signal, and forward it to the digital control.

The raw data is processed in the digital control. Then the processed data is routed to the CRT for display.

The calibration kit is used to calibrate the analyzer system. Calibration ensures the impedance measurement accuracy at the test head terminal.

The power supply in the mainframe supplies all necessary power for the analyzer.

ANALYZER FUNCTIONAL GROUPS

The analyzer consists of six main functional groups: a power supply, a digital control, a source, a receiver, a transducer, and a calibration kit. Each group consists of several major assemblies, and performs a distinct function in the analyzer. (In fact, all the groups are interrelated to some extent and affect each other's performance.)

Power Supply: The power supply functional group consists of the A40 preregulator, A50 DC-DC converter, and the A2 post-regulator. It supplies power to the other assemblies in the analyzer.

Digital Control: The digital control group consists of the A1 CPU, the A30 keyboard, the A32 Instrument BASIC interface, the A51 GSP (Graphics System Processor), the A52 LCD (Liquid Crystal Display), and the A53 FDD (Flexible Disk Drive). These assemblies combine to provide digital control for the analyzer.

Source: The source group consists of the A5 synthesizer, the A4A1 1st LO (1st local oscillator), the A3A1 level vernier, the A3A2 2nd LO (second local oscillator), the A3A3 source, the A7 output attenuator, the A22/A23 DC bias (option 001 only), and the A60 high stability frequency reference (option 1D5 only). The source supplies a phase-locked stimulus signal to the device under test, through the transducer, and supplies the 1st and 2nd local oscillator signals to the receiver. The source supplies a DC bias signal to the device under test when the option 001 is installed.

Receiver: The receiver group consists of the A4A2 receiver RF, and the A6 receiver IF. The receiver measures RF signal inputs, and forwards the measured data to the digital control.

Transducer: The transducer group consists of the A41 TRD Amplifier and the test heads. The transducer interfaces the source and the receiver to the device under test to measure the device impedance.

Calibration Kit: The calibration kit consists of the open, short, 50 Ω, and low-loss capacitor termination. The calibration kit is used to calibrate the analyzer.

The following pages describe the operation of the functional groups.

POWER SUPPLY OPERATION

The power supply functional group consists of the following assemblies:

- A40 Preregulator
- A50 DC-DC Converter
- A2 Post-Regulator

These three assemblies comprise a switching power supply that provides regulated DC voltages to power all assemblies in the analyzer. See Figure 11-2.

The A40 preregulator steps down and rectifies the line voltage, and provide +24 V to the A50 DC-DC converter.

The A50 DC-DC converter contains two switching regulators, and provides the following six power supply voltages.

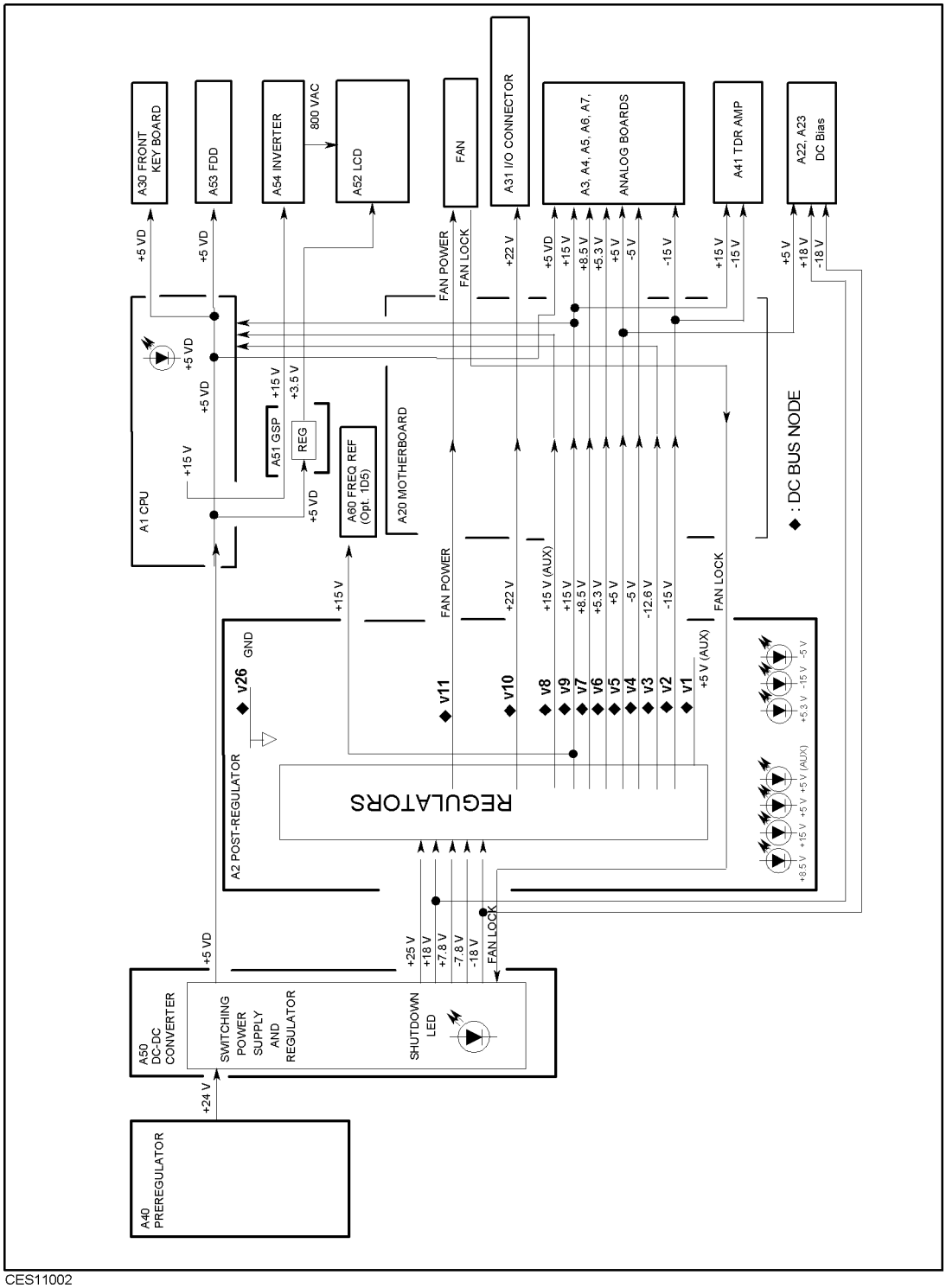
+25 V, +18 V, +7.8 V, +5 VD, −7.8 V, −18 V

The +5 VD (+5 V digital supply) is fully regulated in A50 and is directly supplied to the A1 CPU. The other five power supplies are preregulated in A50 and go to the A2 post-regulator for final regulation. The +18 V and -18 V are directly supplied to A22 DC bias 1/2 also when the option 001 is installed.

A50 receives the FAN LOCK signal from the fan through the A20 motherboard and the A2 post-regulator.

The A2 post-regulator filters and regulates the five power supply voltages from A50. It distributes the following eleven regulated voltages to individual assemblies throughout the analyzer:

FAN POWER (+25 V), +15 V, +15 V (AUX), +8.5, +5.3 V, +5 V, +5 V (AUX), −5 V, −12.6 V, −15 V



CES11002

Figure 11-2. Power Supply Functional Group, Simplified Block Diagram

Line Power Module

The line power module includes the main fuse. The main fuse, which protects the input side of the preregulator from drawing too much line current, is also accessible at the rear panel. See *Power Requirements* in appendix B for the fuse replacement and other power considerations.

A40 Preregulator

The A40 preregulator contains a rectifier and a switching regulator, converts the line voltage to +25 V and provides it to the A50 DC-DC converter.

A50 DC-DC Converter

The A50 DC-DC Converter consists of the two switching regulators (1 and 2). The DC-DC converter provides an LED (visible at the top) to indicate circuit status. See Figure 5-12 in chapter 5. The shutdown LED is turned off when the overcurrent protection circuit activates. The circuit activates when an overcurrent is sensed on the +5 VD power line, when an overcurrent is sensed on the four power supplies (±18 V and ±7.8 V), or when the FAN LOCK signal is sensed. It shuts down the five power supplies of the switching regulators (1 and 2). For A50 to work properly, the +7.8 V must be loaded (approximately 680 ohms, more than 125mW). If it is not, the other preregulated voltages in the A50 DC-DC converter will not be correct.

Switching Regulator 1

Switching regulator 1 converts the +25 V to the regulated +5 VD (digital supply). The +5 VD goes directly to the A1 CPU.

Switching Regulator 2

Switching preregulator 2 converts the +24 V to four DC voltages, +7.8 V, −7.8 V, +18 V, −18 V. The voltages are routed to the A2 post-regulator for final regulation.

Regulated + 5V Digital Supply (+ 5 VD)

The +5VD power supply is fully regulated in the A50 DC-DC converter. It goes directly to the A1 CPU and is supplied to all assemblies requiring a digital +5 V supply through A1, and the A20 motherboard. See Figure 11-2.

A50 Shutdown LED

The A50 shutdown LED is on during normal operation. It turns off when the A50 protective circuits are activated and shut down some power lines. The shutdown LED turns off when one of the following conditions is sensed:

- Overcurrent on +5 VD Power Line.
- Overcurrent on the four power supplies (±18 V and ±7.8 V)
- Fan is not rotating (FAN LOCK signal is sensed).

The fan obtains its power +25 V from A40 preregulator through the A50 DC-DC converter and the A2 post-regulator. When the power is missing, the FAN LOCK signal shuts the switching regulators down and turns the A50 shutdown LED off.

A2 Post-Regulator

The A2 post-regulator consists of seven filters, nine regulators,and the drive circuits for the A7 output attenuator. See Figure 5-13 in chapter 5.

The A2 post-regulator distributes the following eleven power supply voltages to individual assemblies throughout the analyzer. Each of the nine regulators receives the DC voltage pre-regulated in A50 through a filter and converts it to one of the fully regulated constant DC voltages listed below:

FAN POWER	is derived from the +25 V supply from A40. It powers the fan.
+15 V	is derived from the +18 V supply from A50. It powers analog assemblies A3 through A9.
+15 V (AUX)	is derived from the +18 V supply from A50. It powers the three probe power outputs on the front panel.
+8.5 V	is derived from the +15 V supply regulated in the A2 post-regulator. It powers the A3A3 source.
+5.3 V	is derived from the +7.8 V supply from A50. It powers the A3A3 source.
+5 V	is derived from the +7.8 V supply from A50. It powers analog assemblies A3 through A9.
+5 V (AUX)	is derived from the +25 V or +18 V supplies from A50. It powers A2.
–5 V	is derived from the –7.8 V supply from A50. It powers analog assemblies A3 through A7.
–12.6 V	is derived from the –18 V supply from A50. It powers the probe power connector.
–15 V	is derived from the –18 V supply from A50. It powers analog assemblies A3 through A7.

The A2 post-regulator is equipped with a protective shutdown circuit.

The A2 post-regulator provides two LED arrays, visible at the top edge of the A2 post-regulator. Each LED array consists of four LEDs and indicates the status of the seven power supplies.

Shutdown Circuit

Four regulators for power supplies, +15 V, +5 V, –5 V, and –15 V are equipped with the capability of sensing overcurrent, and overvoltage, undervoltage on their output lines. When a regulator senses one of these conditions, it triggers the protective shutdown circuit. The circuit is also triggered by an over temperature condition in A2.

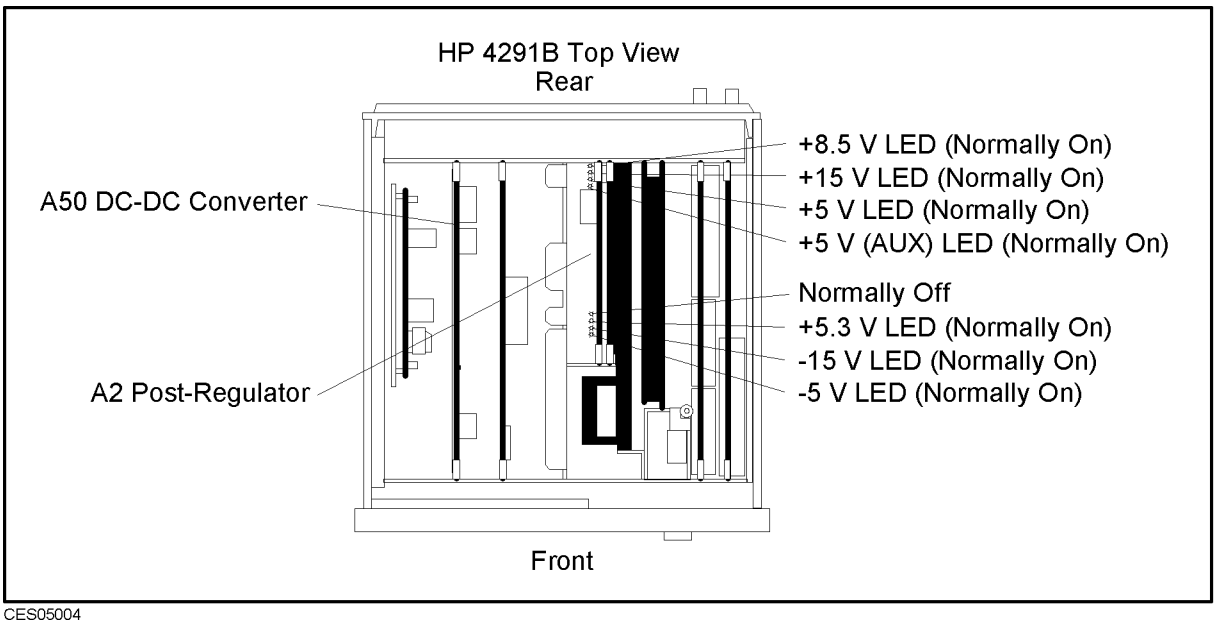
The following power supplies are not shutdown:

FAN POWER, +12.6 V, +15 V (AUX), +5 V (AUX)

The shutdown circuit also provides the shutdown status to the A1 CPU. When the circuit is activated, it triggers the A1 CPU. The A1 CPU checks the shutdown status on the A2 post-regulator and displays a warning message. Then the analyzer stops its operation. Once the analyzer stops the operation, the front-panel keys are disabled. The only way to reset the analyzer is to turn the analyzer power off then on.

Eight Status LEDs

The eight status LEDs on the A2 post-regulator are on during normal operation. They indicate that the correct voltage is present in each supply. See Figure 11-3. If one (or more) of them is off or flashing, there is a problem in the corresponding power supply.



CES05004

Figure 11-3. A2 Eight Status LED

A7 Output Attenuator Drive Circuit

The A2 post-regulator has the drive circuit for the A7 output attenuator. The circuit decodes the control signal from the A1 CPU and generates the following TTL signals:

- A7 output attenuator drive signals (10 dB ON/OFF, 20 dB ON/OFF, 30 dB ON/OFF).

These signals are supplied to A7 through the A20 motherboard.

DIGITAL CONTROL OPERATION

The digital control functional group consists of the following assemblies:

- A1 CPU
- A30 Front Keyboard
- A31 I/O Connector
- A32 I-BASIC Interface
- A51 GSP
- A52 LCD (Liquid Crystal Display)
- A53 FDD (Flexible Disk Drive)

These assemblies provide math processing functions, as well as communications between the analyzer and an external controller and/or peripherals. Figure 11-4 is a simplified block diagram of the digital control functional group.

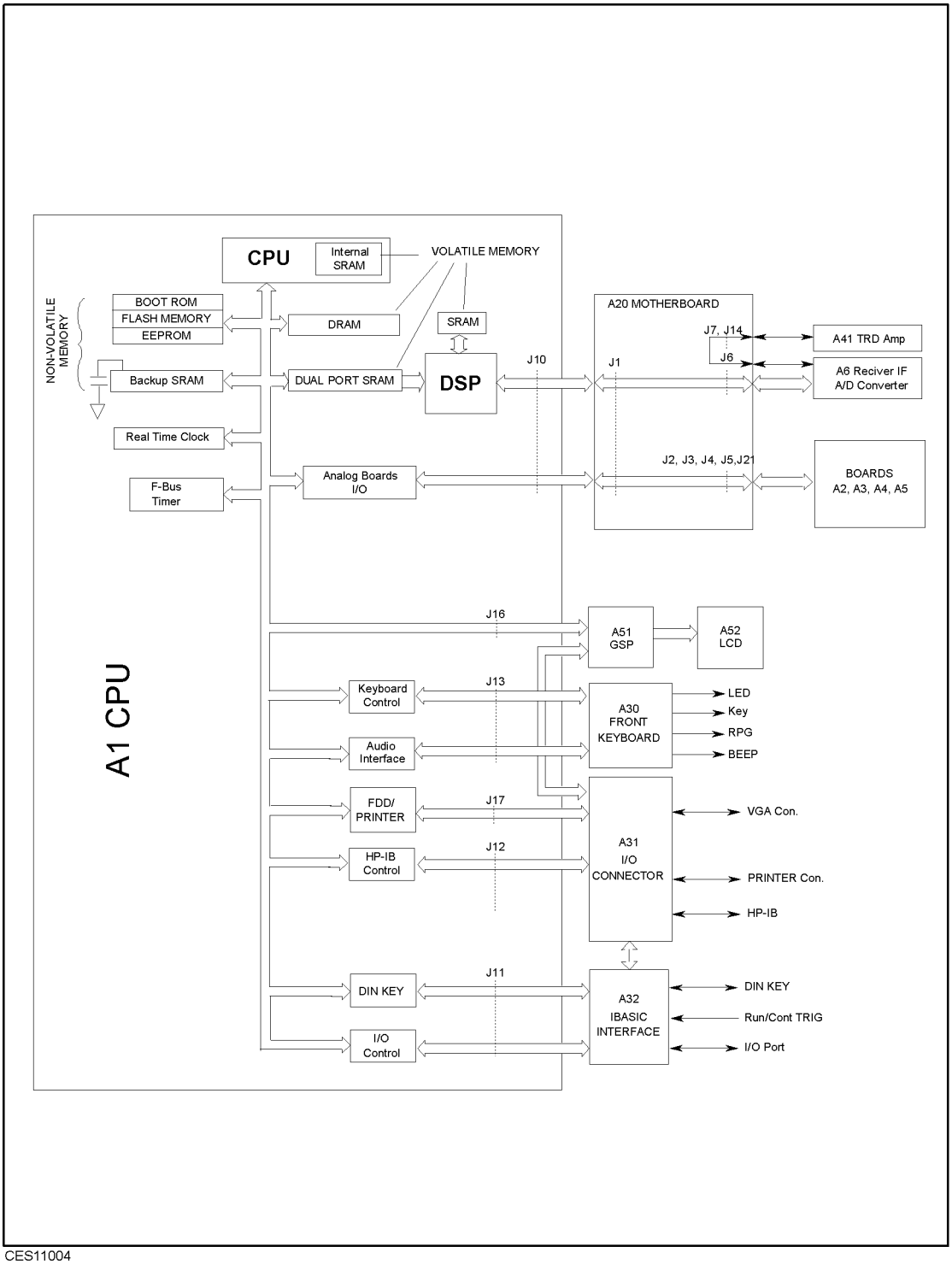


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Figure 11-4. Digital Control Group, Simplified Block Diagram

A1 CPU

The A1 CPU consists of the following circuits and parts (See Figure 11-4):

CPU	central processing unit that controls the analyzer.
DSP	digital signal processor that is used for fast data processing.
Memory storages	consists of BOOT ROMs, Flash Memory, EEPROM, Backup SRAM, DRAM, and Dual Port SRAM. The backup SRAM is powered from a large capacitor that is charged when the analyzer is turned on. Therefore, the SRAM keeps its data at least 72 hours after the analyzer is turned off. The Dual Port SRAM is used for communication between the CPU and DSP.
F-Bus Timer	is used in the frequency bus measurement that is a diagnostic function of the analyzer. For a description of the frequency bus measurement, see the *Service Key Menus* chapter.
Analog Board Interface	interfaces between the CPU and analog assemblies A3 through A7
Keyboard Controller	controls the A30 front-panel keyboard.
Audio Interface	controls the beeper on the A30 front-panel keyboard.
FDD Control	controls the A53 FDD.
HP-IB Control	communicates with the external HP-IB devices through the HP-IB connector on the A31 I/O connector.
External Keyboard Control	interfaces between the CPU and the external keyboard through the mini DIN connector on the A32 I-BASIC Interface.
I/O Control	controls the external devices through the I/O PORT connector on the A32 IBASIC interface. It also interfaces between the CPU and the external inputs through the EXT PROG RUN/CONT connector.

A30 Front-Panel Keyboard

The A30 front-panel keyboard assembly detects your inputs (key inputs and RPG inputs) from the front panel of the analyzer, and transmits them to the keyboard controller on A1.

A31 I/O Connector

The two A31 I/O connector consist of the HP-IB connector, VGA connector, and PRINTER connector. These connectors are connected to the HP-IB controller on A1 through the A20 motherboard.

A32 I-BASIC Interface

The three A32 I/O connectors are the EXT PROG RUN/CONT connector, the I/O Port connector, and the mini DIN Keyboard connector. These connectors are connected to the I/O control and mini DIN control circuit on A1 through the A20 motherboard.

A51 GSP

The A51 GSP (graphics system processor) provides an interface between the A1 CPU and the A52 LCD. The A1 CPU converts the formatted data to GSP commands and writes them to the A51 GSP. The A51 GSP processes the data to obtain the necessary signals and sends these signals to the A52 LCD.

The A51 GSP receives two power supply voltages: +5 VD, which is used for data processing and converted to +3.3 V, and +15 V, which is passed on the A54 Inverter. The +3.3 V goes to the A52 LCD. See Figure 5-1 for more details.

A52 LCD (Liquid Crystal Display)

The A52 LCD is a 8.4 TFT Color LCD, receives a high voltage (800 to 1000 VAC) from the A54 Inverter as backlight power and the digital horizontal and the vertical signals from the A51 GSP.

A53 FDD

The analyzer has a built-in, 3-1/2 inch FDD (Flexible Disk Drive) on the front panel. It uses 2 high density or 2 double density 3-1/2 inch flexible disks. The A53 FDD stores and retrieves data to and from the disk.

A54 Inverter

The A54 Inverter is located in the LCD module on the front panel assembly. The A54 receives +15 V from A1 CPU and provides a high voltage (800 to 1000 VAC) to the backlight of the LCD. See Figure 5-1 for more details.

SOURCE THEORY

The three functional subgroups of the source group are the synthesizer, the stimulus, and the DC bias.

The synthesizer subgroup generates the 40 MHz reference frequency, the 1st local oscillator signal (2.05958 GHz to 3.85858 GHz), and the second local oscillator signal (2.08 GHz). These signals are used in the stimulus signal subgroup in both the source functional group and in the receiver functional group. There are two synthesizer operation modes used in generating the first local oscillator signal, the single-loop mode and the triple-loop mode. The single-loop mode is used to generate the 1st local oscillator signal when the frequency span setting of the analyzer is wider than 45 MHz. At frequency span settings $\leq$ 45 MHz, the triple-loop mode is used to generate the 1st local oscillator signal with low phase noise.

The stimulus subgroup generates a stable and accurate stimulus signal. This signal is a CW or swept signal between 1 MHz to 1.8 GHz with a power level from −60 dBm to +20 dBm.

The DC bias subgroup generates a 0 to ± 40 V DC bias voltage, and 0 to ± 100 mV DC bias current.

Figure 11-5 shows the simplified block diagram of the source functional group. The source group consists of the following assemblies:

- A5 Synthesizer
- A4A1 1st LO
- A60 High Stability Frequency Reference (Option 1C2)
- A3A1 Source Vernier
- A3A2 2nd LO
- A3A3 Source
- A7 Output Attenuator
- A22 DC Bias 1/2
- A23 DC Bias 2/2

The first three assemblies and part of the A3A2 2nd LO belong to the synthesizer subgroup. The next four assemblies belong to the stimulus subgroup. A3A2 contains the second local oscillator and the source first mixer. The second local oscillator is part of the synthesizer subgroup. The source first mixer is part of the stimulus subgroup. The last two assemblies belong to the DC bias subgroup.

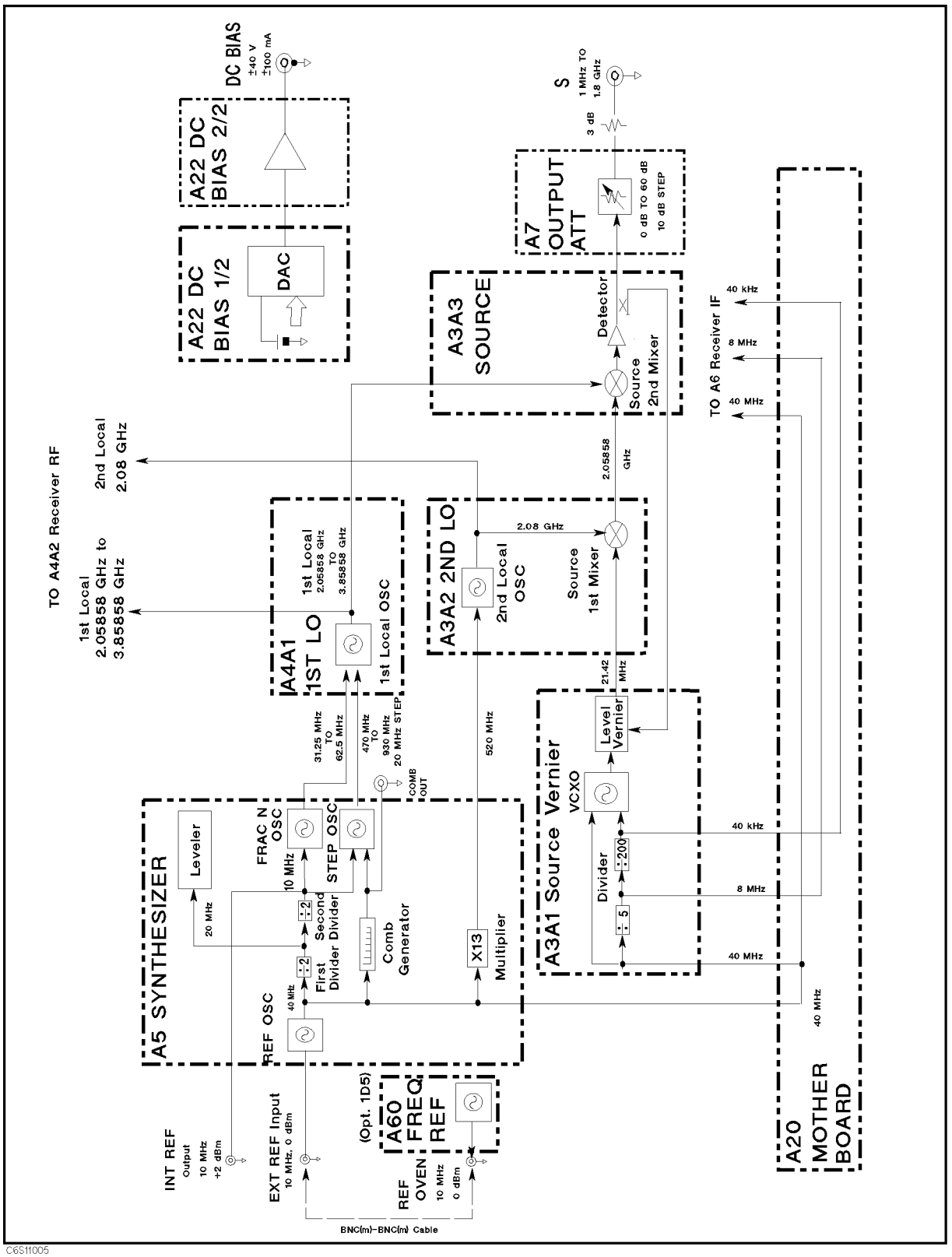

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Figure 11-5. Source Simplified Block Diagram

A5 Synthesizer

The A5 synthesizer provides a 40 MHz reference frequency, an INT REF signal, a FRAC N OSC signal, a STEP OSC signal, and a 520 MHz signal.

The 40 MHz reference signal is supplied to the A3A1 level vernier and the A6 receiver IF and is used as the reference signal. The FRAC N OSC and the STEP OSC signals are supplied to the A4A1 1st LO and are used to generate the 1st local oscillator signal. The 520 MHz signal is supplied to the A3A2 2nd LO and is used to generate the second local oscillator signal.

The A5 Synthesizer consists of the following circuits:

- REF OSC (Reference Oscillator)
- FRAC N OSC (Fractional N Oscillator)
- STEP OSC (Step Oscillator)
- × 13 Multiplier

REF OSC

The REF OSC generates stable 10 MHz and 40 MHz reference frequencies. It does this by dividing the output of a 40 MHz VCXO (voltage control crystal oscillator) as required. The 40 MHz reference signal is supplied to the A3A1 level vernier. The 10 MHz reference frequency is routed to the INT REF Output connector on the rear panel.

When a 10 MHz external reference signal is applied to the EXT REF Input connector on the rear panel, the REF OSC output signals are phase locked to the external reference signal.

The REF OSC is a phase locked oscillator and contains a 40 MHz VCXO, a phase detector, and three 1/2 dividers. See Figure 11-10. When the 10 MHz external reference signal is applied to the EXT REF Input connector on the rear panel, the reference frequency is divided by two. It is then compared with the VCXO frequency ($\mathbf{F_{vcxo}}$) divided by eight in the phase detector. Phase locking imposes the condition of 10 MHz/2 = $\mathbf{F_{vcxo}}$/8. Therefore, the output frequency ($\mathbf{F_{vcxo}}$) is locked to 40 MHz.

A detector circuit detects the external reference input signal and sends the status to the A1 CPU. Then the A1 CPU displays a message (**ExtRef**) on the CRT. In addition, an unlock detector monitors the control voltage to the VCXO. When the control voltage is out of limits, the detector sends the status to the A1 CPU. Then the A1 CPU causes the message **CAUTION: PHASE LOCK LOOP UNLOCKED** to be displayed.

The *40 MHz Reference Oscillator Frequency Adjustment* adjusts the VCXO to lock to the 40 MHz when the external reference signal is not applied.

FRAC N OSC

The FRAC N OSC (Fractional N Oscillator) generates a swept signal of 31.25 MHz to 62.5 MHz with a high frequency resolution. The signal is supplied to the A4A1 1st LO and is used to generate the swept 1st local oscillator signal.

The FRAC N OSC is a phase locked oscillator. The output signal is phase locked to the 10 MHz reference signal of the REF OSC. The oscillator contains a 31.25 MHz to 62.5 MHz VCO, a phase detector, and a fractional N divider (N.F. divider: 1/**in**teger.**f**raction). See Figure 11-10.

The 10 MHz reference signal from the REF OSC is applied to the phase detector through the 1/10 divider. The reference signal is then compared with the VCO frequency ($\mathbf{F_{vco}}$) divided by the fractional N divider in the phase detector. Phase locking imposes the condition of 10 MHz/10 = $\mathbf{F_{vco}}$/N.F. Therefore, the output frequency ($\mathbf{F_{vco}}$) is locked to 1 MHz × N.F.

The fractional N divider is a dedicated divider used to generate the high frequency resolution signal. It divides the signal frequency by a real value (N.F.). The resolution of the fractional part F is 3.55×10^{-15} ($= 1/2^{48}$). Therefore, the FRAC N OSC generates a swept signal with

3.55 nHz (1 MHz × 3.55 × 10^{-15}) frequency resolution. The fractional N divider is controlled by the A1 CPU and the A6 Receiver IF.

STEP OSC

The STEP OSC (Step Oscillator) generates a CW signal between 470 MHz and 910 MHz in 20 MHz steps. The signal is supplied to the A4A1 1st LO and is used to generate the 1st local oscillator signal (only in the triple-loop mode). The output signal frequency depends on the frequency center setting as shown in Table 11-1.

Table 11-1. STEP OSC Frequency

HP 4291B Center Frequency	STEP OSC Frequency
1 MHz ≤ Center < 48.92 MHz	470 MHz
48.92 MHz ≤ Center < 128.92 MHz	490 MHz
128.92 MHz ≤ Center < 208.92 MHz	510 MHz
208.92 MHz ≤ Center < 288.92 MHz	530 MHz
288.92 MHz ≤ Center < 368.92 MHz	550 MHz
368.92 MHz ≤ Center < 448.92 MHz	570 MHz
448.92 MHz ≤ Center < 528.92 MHz	590 MHz
528.92 MHz ≤ Center < 608.92 MHz	610 MHz
608.92 MHz ≤ Center < 688.92 MHz	630 MHz
688.92 MHz ≤ Center < 768.92 MHz	650 MHz
768.92 MHz ≤ Center < 848.92 MHz	670 MHz
848.92 MHz ≤ Center < 928.92 MHz	690 MHz
928.92 MHz ≤ Center < 1008.92 MHz	710 MHz
1008.92 MHz ≤ Center < 1088.92 MHz	730 MHz
1088.92 MHz ≤ Center < 1168.92 MHz	750 MHz
1168.92 MHz ≤ Center < 1248.92 MHz	770 MHz
1248.92 MHz ≤ Center < 1328.92 MHz	790 MHz
1328.92 MHz ≤ Center < 1408.92 MHz	810 MHz
1408.92 MHz ≤ Center < 1488.92 MHz	830 MHz
1488.92 MHz ≤ Center < 1568.92 MHz	850 MHz
1568.92 MHz ≤ Center < 1648.92 MHz	870 MHz
1648.92 MHz ≤ Center < 1728.92 MHz	890 MHz
1728.92 MHz ≤ Center < 1800.00 MHz	910 MHz

The STEP OSC consists of a comb generator and a phase locked oscillator that is phase locked to the 10 MHz reference signal of the REF OSC.

The comb generator receives the 40 MHz reference signal from the REF OSC and multiples the fundamental signal into a comb of harmonic frequencies (40 MHz × N). The level of the harmonics is adjusted in the *Comb Generator Adjustment*.

The phase locked oscillator consists of a 470 MHz to 910 MHz VCO, a phase detector, a mixer, a pretune DAC and ±1 converters. See Figure 11-10. The VCO frequency ($\mathbf{F_{vco}}$) is mixed with the comb generator output in the mixer. The mixer produces multiple harmonics ($\mathbf{F_{vco}}$ ± 40 MHz × N) through the LPF (low pass filter). The mixer output is compared with the 10 MHz reference signal in the phase detector. Phase locking imposes the condition of 10 MHz = $\mathbf{F_{vco}}$ ± 40 MHz × N, and the loop locks to the nearest 40 MHz harmonic satisfying that condition. The initial frequency ($\mathbf{F_{vco}}$) is set to the desired harmonic frequency of **40 MHz × N** (N = 12 to 23) using the pretune DAC. This locks the output frequency ($\mathbf{F_{vco}}$) to the desired **40 MHz × N ± 10 MHz**

selection of the frequencies listed in Table 11-1. The polarity of the 10 MHz offset is controlled by the ±1 converters in the loop.

An unlock detector monitors the control voltage to the VCO. When the control voltage is out of limits, the detector sends the status to the A1 CPU. The A1 CPU causes the message **CAUTION: PHASE LOCK LOOP UNLOCKED** to be displayed.

The pretune DAC values are predefined by performing the *Step Pretune Correction Constants* and are stored in the EEPROM in the A1 CPU.

Multiplier (× 13)

The multiplier receives the 40 MHz reference signal and generates a 520 MHz signal. This signal is supplied to A3A2 2nd LO and is used to generate the second local oscillator signal. See Figure 11-10. The 520 MHz signal level is adjusted in the *520 MHz Level Adjustment*.

A4A1 1st LO

The A4A1 1st LO generates the swept 1st local oscillator signal 2.05958 GHz to 3.85858 GHz with 1 mHz resolution. The sweep range depends on the start and stop (or center and span) settings of the analyzer. The signal frequency sweeps between the start frequency + 2.05958 GHz to the stop frequency + 3.85858 GHz.

The 1st local oscillator signal is supplied to the A3A3 source and the A4A2 receiver RF. In A3A3, the local oscillator signal is used to convert the 2.05858 GHz IF (intermediate frequency) signal to the 1 MHz to 1.8 GHz RF signal. A4A2 also uses the first local to convert the RF input signal to the IF signal.

In addition, the A4A1 1st LO decodes two digital control signals for the A4A2 Receiver RF, and the decoded signals are supplied to A4A2.

1st Local OSC Circuit

The 1st local oscillator circuit is a phase locked oscillator. The output signal is phase locked to the FRAC N OSC output signal. The oscillator contains a 2.05958 GHz to 3.85858 GHz VCO, a phase detector, a 1/4 divider, a mixer, a 1/16 divider, and a single/triple switch. See Figure 11-10.

The single/triple switch is for the single/triple mode and switches the VCO signal to one of the mixers and the 1/16 divider.

An unlock detector monitors the control voltage to the VCO. When the control voltage is out of the limits, the detector sends the status to the A1 CPU. The A1 CPU causes the message **CAUTION: PHASE LOCK LOOP UNLOCKED** to be displayed.

Single-Loop Operation at Frequency Spans > 45 MHz. In the single-loop mode, the VCO signal loops back to the phase detector through the 1/4 divider and the 1/16 divider. The VCO frequency ($\mathbf{F_{vco}}$) is divided by 64 and then compared with the FRAC N OSC signal frequency ($\mathbf{F_{frac}}$) (31.25 MHz to 62.5 MHz) in the phase detector. Phase locking imposes the condition of $\mathbf{F_{frac}} = \mathbf{F_{vco}}$ /64. Therefore, the output frequency ($\mathbf{F_{vco}}$) is locked to $\mathbf{F_{frac}} \times 64$. The $\mathbf{F_{vco}}$ sweeps from 2 GHz (31.25 MHz × 64) to 4 GHz (62.5 MHz × 64) according to the FRAC N OSC; swept signal. The frequency range actually used in the analyzer is 2.05958 GHz (at a measurement frequency 1 MHz) to 3.85858 GHz (at a measurement frequency 1.8 GHz).

Triple-Loop Operation at Frequency Spans ≤ 45 MHz. In the triple-loop mode, the VCO signal loops back to the phase detector through the 1/4 divider and the mixer. The VCO frequency ($\mathbf{F_{vco}}$) is mixed with the STEP OSC output ($\mathbf{F_{step}}$) in the mixer. The mixer then produces the shifted frequency of $\mathbf{F_{vco}}/4 - \mathbf{F_{step}}$. The mixer output is compared with the FRAC N OSC output signal in the phase detector. Phase locking imposes the condition of $\mathbf{F_{frac}} = \mathbf{F_{vco}}/4 - \mathbf{F_{step}}$. Therefore, the output frequency $\mathbf{F_{vco}}$ is locked to $\mathbf{F_{frac}} \times 4 + \mathbf{F_{step}} \times 4$. The

$\mathbf{F_{vco}}$ sweeps over the appropriate range determined by the start and stop setting according to the $\mathbf{F_{frac}}$.

The $\mathbf{F_{step}}$ is determined by the center frequency of the analyzer as shown in Table 11-1. The $\mathbf{F_{frac}}$ sweeps between {(start frequency + 2.05958 GHz)/4 – $\mathbf{F_{step}}$}/4 to {(stop frequency + 2.05958 GHz)/4 – $\mathbf{F_{step}}$}/4.

A3A1 Source Vernier

The A3A1 source vernier generates the level-controlled 21.42 MHz IF signal, an 8 MHz reference signal, and a 40 kHz reference signal.

The 21.42 MHz signal is supplied to the A3A2 2nd LO and converted to a 2.05858 GHz IF signal through the source first converter. The 8 MHz and 40 kHz signals are supplied to the A6 receiver IF and used as reference signals.

The A3A1 level vernier consists of the following circuits:

- Divider
- Source Oscillator
- Level Vernier

Divider

The divider contains a 1/5 divider and a 1/200 divider. The 40 MHz reference frequency from the A5 synthesizer is down converted to 8 MHz and 40 kHz through the two dividers. The two signals are then supplied to the A6 receiver IF through the A20 motherboard.

Source OSC

The source OSC (source oscillator) is a phase locked oscillator. The output signal is phase locked to the 40 kHz frequency of the divider output. The oscillator generates the 85.68 MHz signal. The signal is divided by the 1/4 divider. The resulting 21.42 MHz signal is supplied to the level vernier circuit.

The oscillator contains an 85.68 MHz VCXO, a phase detector, a 1/2 divider, a mixer, and a 1/71 divider. See Figure 11-10. The VCO frequency ($\mathbf{F_{vco}}$) is divided by 2 and mixed with the 40 MHz reference frequency in the mixer. The mixer then produces a shifted frequency ($\mathbf{F_{vco}}$/2 – 40 MHz). The mixer output is divided by 71 and then compared with the 40 kHz reference signal in the phase detector. Phase locking imposes the condition of 40 kHz = ($\mathbf{F_{vco}}$/2 – 40 MHz)/71. Therefore, the output frequency ($\mathbf{F_{vco}}$) is locked to 85.68 MHz (= (40 kHz × 71 + 40 MHz) × 2).

The VCXO is optimized by the “Source VCXO Adjustment.”

Level Vernier

The level vernier controls the level of the 21.42 MHz CW signal from the source OSC. The signal is routed to the output connector on the front panel through the A3A2 2nd LO, the A3A3 source, and the A7 Output Attenuator.

The level vernier consists of a level DAC and a level vernier. See Figure 11-10.

The level vernier changes the 21.42 MHz signal level according to the DAC output level. The DAC output level is set according to the predefined data in the EEPROM on the A1 CPU. The data is stored by performing the *OSC Level Correction Constants*.

A3A2 2nd LO

The A3A2 2nd LO generates the second local oscillator signal (a 2.08 GHz CW signal) and converts the 21.42 MHz signal from the A3A1 level vernier to a 2.05858 GHz IF signal by mixing the 21.42 MHz and the second local oscillator signal.

The 2.05858 GHz IF signal is supplied to the A3A3 source and then converter to a swept RF signal. The second local oscillator signal is supplied to the A4A2 receiver RF.

The A3A2 2nd LO consists of the following circuits:

- 2nd LO
- Source First Mixer

2nd LO

The 2nd Local oscillator circuit is a phase locked oscillator. The output signal is phase locked to the 520 MHz frequency from the A5 synthesizer. The oscillator generates a 2.08 GHz signal. The signal is supplied to the source first mixer and the A4A1 receiver RF.

The oscillator contains a 1.04 GHz VCO, a phase detector, and a 1/2 divider. See Figure 11-10. The VCO frequency ($\mathbf{F_{vco}}$) is divided by 2 and then compared with the 520 MHz reference signal in the phase detector. Phase locking imposes the condition of 520 MHz = $\mathbf{F_{vco}}/2$. Therefore, the output frequency ($\mathbf{F_{vco}}$) is locked to 1.04 GHz (= 520 MHz × 2). Then the signal frequency is converted to 2.08 GHz by the doubler.

The 520 MHz reference signal contains 40 MHz harmonics because it is generated by multiplying the 40 MHz reference signal in the A5 synthesizer. The *Second Local PLL Adjustment* adjusts the 2nd LO to lock to the 520 MHz harmonic, rather than the neighboring harmonics (480 MHz or 560 MHz).

An unlock detector monitors the control voltage to the VCO. When the control voltage is out of the limits, the detector sends the status to the A1 CPU. The A1 CPU causes the message **CAUTION: PHASE LOCK LOOP UNLOCKED** to be displayed.

Source First Mixer

The 21.42 MHz CW signal from the A3A1 level vernier is mixed with the 2.08 GHz second local oscillator signal through the first source mixer. Then the signal is converted to a 2.05858 GHz CW signal through the BPF (band pass filter). The 2.05858 GHz signal is supplied to the A3A3 source.

A3A3 Source

The A3A3 source generates a stable and accurate RF signal. This signal is a CW or swept signal between 1 MHz to 1.8 GHz, with a power level from −10 dBm to +20 dBm. The RF signal is supplied to the A7 output attenuator. The A3A3 source consists of the following circuits (see Figure 11-10):

- Source Second Mixer
- Source Amplifier
- Level Detector

The 2.05858 GHz IF signal from the A3A2 2nd LO is applied to the source second mixer. It is then converted to the CW or swept RF signal (1 MHz to 1.8 GHz) by mixing with the CW or swept 1st local oscillator signal (2.05958 GHz to 3.85858 GHz) from the A4A1 1st LO. The RF signal is amplified with a constant gain through the source amplifier. It is then supplied to the A7 output attenuator through the level detector. The level detector loops the RF signal level back to the A3A1 level vernier.

A7 Output Attenuator

The A7 output attenuator is a 10 dB step attenuator from 0 dB to 60 dB. A7 consists of three segments (10 dB, 20 dB, and 30 dB). Attenuation from 0 dB to 60 dB is obtained by combining one (or more) of the three segments. Each segment is activated by the TTL signals from the A2 post-regulator.

Table 11-2 shows the relationship between the oscillator level setting and the A7 setting.

Table 11-2. Osc Level Setting vs. A7 Output Attenuator Setting

Osc Level	A7 Attenuation
0.22 Vrms < Osc ≤ 1.0 Vrms[1]	0 dB
70 mVrms < Osc ≤ 0.22 Vrms	10 dB
22 mVrms < Osc ≤ 70 mVrms	20 dB
7.0 mVrms < Osc ≤ 22 mVrms	30 dB
2.2 mVrms < Osc ≤ 7.0 mVrms	40 dB
0.70 mVrms < Osc ≤ 2.2 mVrms	50 dB
0.20 mVrms < Osc ≤ 0.70 mVrms	60 dB

1 Osc ≤ 0.5 Vrms for frequency > 1 GHz

A22/A23 DC Bias

The A22 DC bias 1/2 and A23 DC bias 2/2 are DC bias sources that provide constant bias voltage up to 40 V, and constant bias current up to 100 mA.

The DC bias source has two operational modes, a voltage setting mode and a current setting mode. In the voltage setting mode, the bias level is set by voltage and the bias limit is set by current. In this mode, the bias source provides a constant bias voltage until the bias current rises above the current limit setting. In the current setting mode, the bias level is set by current and the bias limit is set by voltage.

A22 consists of three DACs that generate bias voltage control and bias current control signals. The bias voltage control signal is 1/10 of the bias voltage level (or limit) setting. The bias current control signal is 100/9 [V/A] of the bias current level (or limit) setting [A]. The bias voltage control signal is output from the voltage DAC and the bias current control signal is output from the current DAC. The gain DAC is used to adjust the voltage step magnitude. These DAC output levels are set according to the predefined data in the EEPROM on the A1 CPU. This data is stored by performing the *DC Bias Level Correction Constants* procedure.

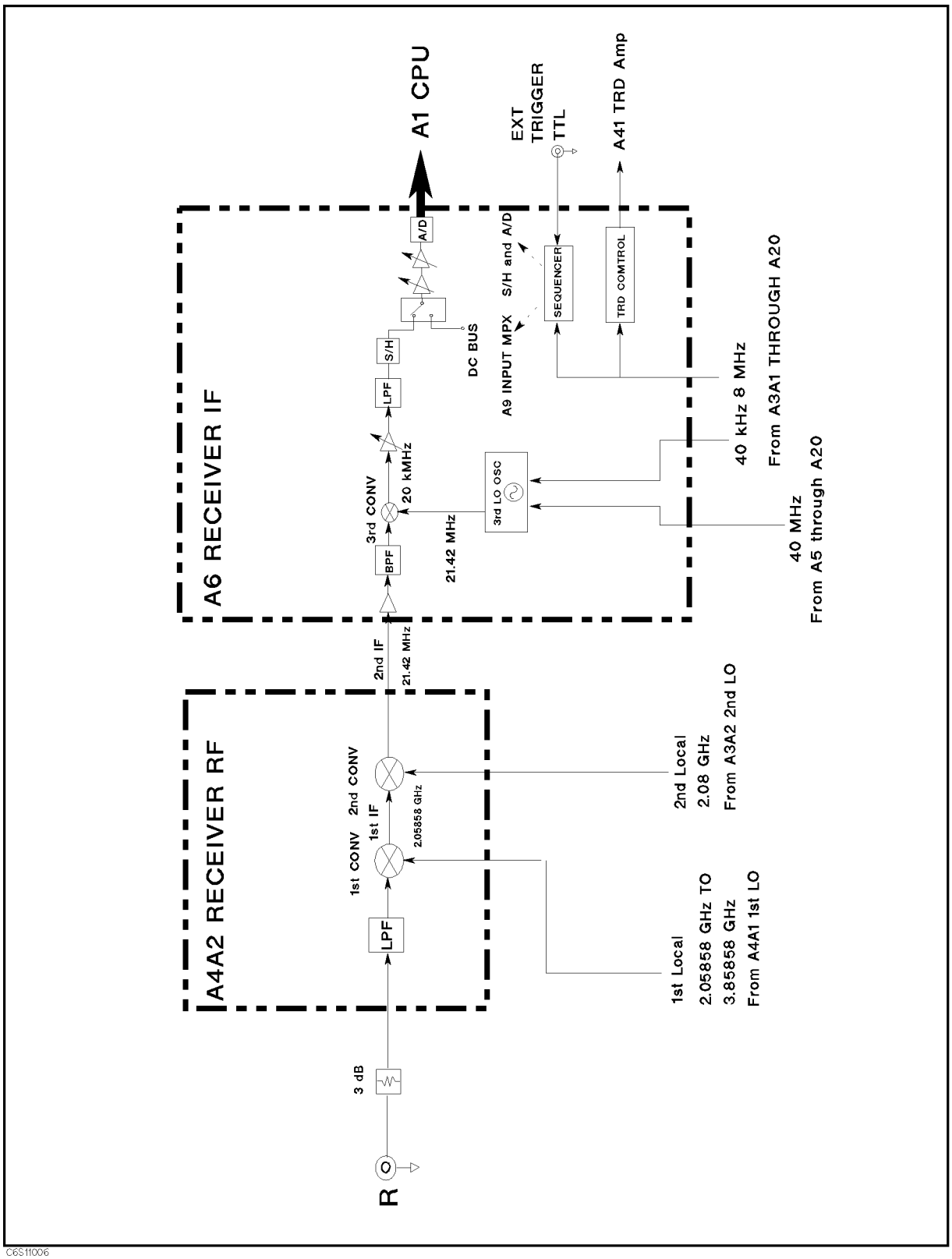
A23 is a power amplifier with a feedback loop. A23 provides DC bias voltage and current, according to the control signals from A22. In the voltage setting mode, A23 generates a bias voltage of (bias voltage control signal) × 10. In the current setting mode, A23 generates a bias current of (bias current control signal [V]) × 9/100 [A/V].

RECEIVER THEORY

The receiver receives the RF signal from the transducer group and converts the signal to digital data. The RF signal is converted to the 1st IF (intermediate frequency), then to 2nd IF, and finally to the 3rd IF. The 3rd IF is converted to a digital signal using A/D converter.

Figure 11-6 shows the simplified block diagram of the receiver functional group. The receiver group consists of the following assemblies:

- A4A2 Receiver RF
- A6 Receiver IF



C6S11006

Figure 11-6. Receiver Simplified Block Diagram

A4A2 Receiver RF

The A4A2 receiver RF converts the RF input signal from the transducer group to the 21.42 MHz 2nd IF. The 2nd IF is routed to the A6 receiver IF.

The A4A2 receiver RF consists of the following circuits (see Figure 11-11):

- 1st Converter
- 2nd Converter

In the first converter, the RF signal (1 MHz to 1.8 GHz) is mixed with the 1st local oscillator signal (2.05958 GHz to 3.85858 GHz) from A4A1 and then converted to the 2.05858 GHz 1st IF through the band pass and low pass filters.

In the second converter, the 1st IF is mixed with the 2.08 GHz second local oscillator signal from A3A2. This converts it to the 21.42 MHz second IF through the low pass filters.

The second IF signal is routed to A6 receiver IF.

A6 Receiver IF

The A6 Receiver IF converts the 21.42 MHz 2nd IF from A4A2 to the final 3rd IF. The 3rd IF is then converted to a digital value in the A/D converter. The digital signal is routed to the DSP on the A1 CPU.

The A6 receiver IF consists of the following circuits (see Figure 11-11):

- Third Local Oscillator
- Third Converter
- Sample/Hold and A/D Converter
- Gains X, Y, and Z

Third Local Oscillator

The third local oscillator is a phase locked oscillator. The output signal is phase locked to the 40 kHz frequency of the divider output. The oscillator generates the 85.6 MHz signal. The signal divided by the 1/4 divider. The resulting 21.4 MHz signal is supplied to the third converter.

The oscillator contains an 85.6 MHz VCXO, a phase detector, a 1/2 divider, a mixer, and a 1/70 divider. See Figure 11-10. The VCXO frequency ($\mathbf{F_{vcxo}}$) is divided by 2 and mixed with the 40 MHz reference frequency in the mixer. The mixer then produces a shifted frequency ($\mathbf{F_{vcxo}}/2 - 40$ MHz). The mixer output is divided by 70 and then compared with the 40 kHz reference signal in the phase detector. Phase locking imposes the condition of 40 kHz = ($\mathbf{F_{vcxo}}/2 - 40$ MHz)/70. Therefore, the output frequency ($\mathbf{F_{vcxo}}$) is locked to 85.6 MHz (= (40 kHz × 70 + 40 MHz) × 2).

An unlock detector monitors the control voltage to the VCXO. When the control voltage is out of limits, the detector sends the status to the A1 CPU. Then the A1 CPU causes the message **CAUTION: PHASE LOCK LOOP UNLOCKED** to be displayed.

The VCXO is optimized by the "Third Local VCXO Adjustment."

Third Converter

In the third converter, the 21.42 MHz second IF is mixed with the 21.4 MHz third local signal and then converted to the final 20 kHz third IF.

The third converter is an image rejection mixer that rejects the 20 kHz signal converted from 21.38 MHz and 21.4 MHz. It also rejects errors caused by the 21.38 MHz component mixed into the second IF.

In the mixer, the 21.42 MHz second IF is divided into two paths (0° path and 90° path) and then mixed with the 90° phase different 21.4 MHz signals. Therefore, the 90° phase different 20 kHz signals are converted. The 90° path 20 kHz lags the 0° path 20 kHz by 90°s. Then the two phase shifters shift the 90° path 20 kHz forward by 90°. Therefore, the 90° path and the 0° path signals are in phase. Then the third IF signal is generated by adding the two 20 kHz signals that are in phase.

When 21.38 MHz signal is applied to the mixer. The 90° path mixer output 20 kHz forwards that of 0° path by 90°. Therefore, the 90° path phase sifter output 20 kHz forwards that of 0° path by 180°. These two signals are canceled by being added to each other.

Sample/Hold and A/D Converter

The 3rd IF is sampled and held in the Sample/Hold circuit. The hold signal is applied to the A/D converter through the A/D multiplexer and then converted to a digital value. The A/D multiplexer multiplexes the hold signal and the DC bus.

The DC bus is a single multiplexed line that networks 26 nodes within the analyzer. When the DC bus is connected to the A/D converter, the A/D converter is used to measure the voltage at a selected node within the analyzer. For more information about the DC bus measurement, see Chapter 10.

The analyzer has a 16 bit A/D converter capable of sampling at 100 ks/s. In this application, it samples at the rate of 80 ks/s. The sequencer consists of four GALs (gate array logic) ICs that are used as follows:

- Timing generator for the sample/hold the A/D converter.
- Timing generator/Gate shaper for the real time gated analysis.
- Timer driver/Input multiplexer driver/Frequency increment driver (controlling A5 FRAC N OSC).
- Decoder for the control signal from the A1 CPU.

Gains X, Y, and Z

The gains X (0 dB/6 dB/12 dB), Y (0 dB/6 dB/12 dB/18 dB), and Z (0 dB/2 dB/4 dB/18 dB) are variable amplifiers.

These amplifiers are used to optimize the IF gain (total gain through the 1st/2nd/3rd IF signal path) in order to use the A/D converter's widest possible dynamic range. The analyzer coarsely measures device impedance to determine the amplifiers' gains, then measures device impedance with optimum gain setting.

TRANSDUCER THEORY

The transducer group receives the stimulus signal from the source group and applies it to the device under test (DUT). At the same time, the transducer group senses two signals that represent the voltage across the DUT and the current through the DUT, multiplexes these signals, and applies them to the receiver group.

Figure 11-7 is the transducer group simplified block diagram. The transducer group consists of the following assemblies:

- Test Heads
- A41 TRD Amp

The A41 TRD amp is a main part of the test station.

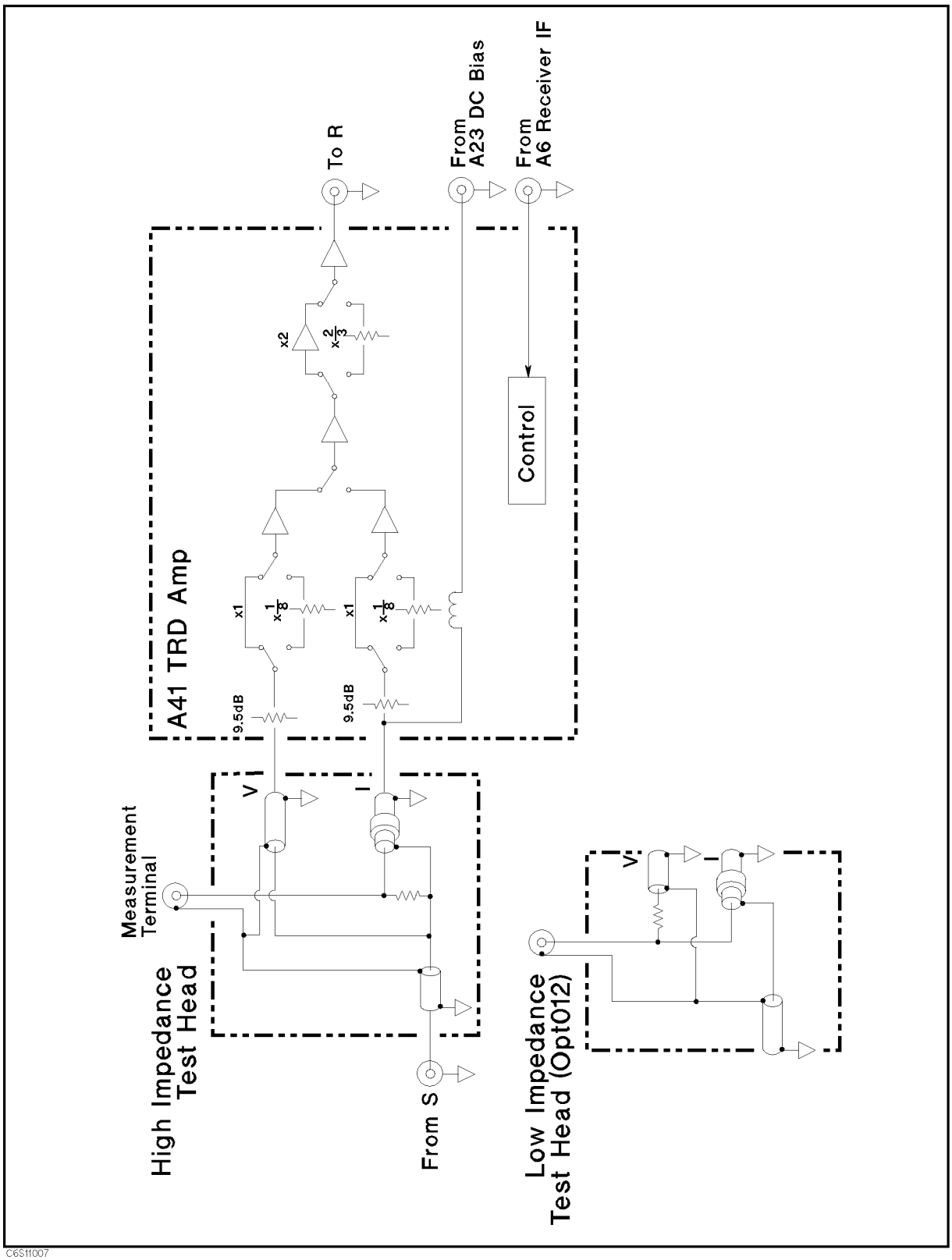


Figure 11-7. Transducer Simplified Block Diagram

Test Heads

There are two types of the test heads. One is a high impedance test head and the other is a low impedance test head. (See Figure 11-7.) Having two types of test heads expands the analyzer's high accuracy impedance measurement range.

When the high impedance test head is used, the analyzer operates as shown in Figure 11-8.

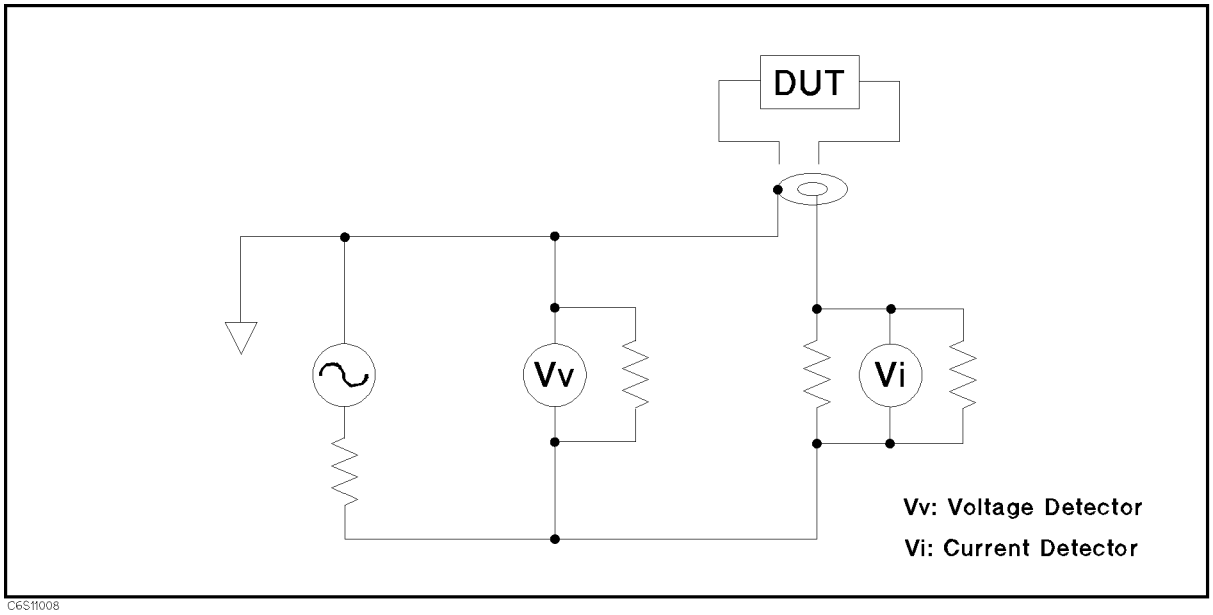


Figure 11-8. High Impedance Measurement Block Diagram

The high impedance test head configuration is used for measuring high impedance devices. In high impedance device measurements, the current through the device changes according to the device impedance and the voltage across the device is almost constant. Therefore, the current measurement is the key for high impedance measurement. The high impedance test head configuration measures the current through the device because all the current through the device flows through the current detector as shown in Figure 11-8.

When a low impedance test head is used, the analyzer operates as shown in Figure 11-9.

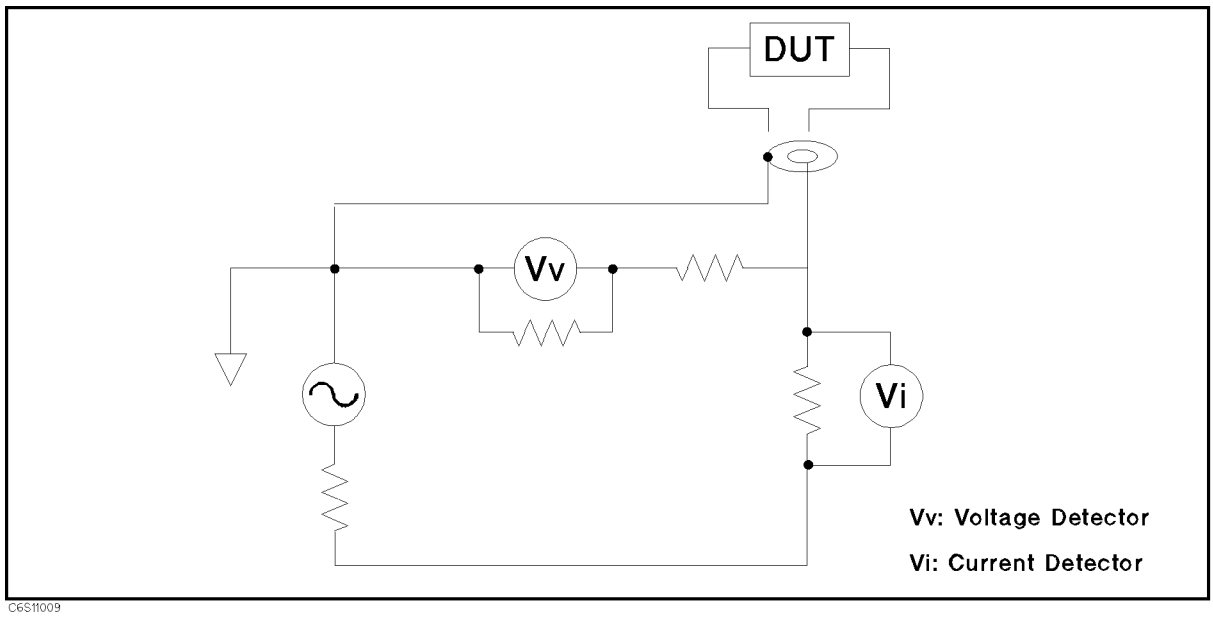


Figure 11-9. Low Impedance Measurement Block Diagram

The low impedance test head configuration is suited for measuring low impedance devices. In low impedance device measurements, the voltage across the device changes according to the device impedance, and the current through the device is almost constant. Therefore, the voltage measurement is the key for low impedance measurement. The low impedance test head configuration is suited for measuring the voltage across the device because the voltage detector is directly connected to the device as shown in Figure 11-9.

A41 TRD Amplifier

The A41 TRD amplifier receives V and I signals from the test head and transmits the signals to the receiver group. The TRD amplifier multiplexes and normalizes the signals so that the signals can be measured accurately with one receiver.

The A41 TRD amplifier consists of the following circuits:

- Gv/Gi ATT and Level Normalizer
- V/I Multiplexer
- Control

Gv/Gi ATT and Level Normalizer

The Gv ATT (×1, ×1/8), Gi ATT (×1, ×1/8), and Level Normalizer (×2, ×2/3) consists of attenuators, an amplifier, and semiconductor switches.

Gv/Gi ATT settings are determined from the oscillator level and device impedance. The level normalizer setting is determined from the oscillator level. The analyzer coarsely measures device impedance to determine Gv/Gi ATT settings, then measures the device impedance with an optimum gain setting. Table 11-3 shows the gain settings.

Table 11-3. TRD Amplifier Gain Settings

Oscillator Level	Normal		Hi-Z[1]		Lo-Z[2]		Level Normalizer
	Gv	Gi	Gv	Gi	Gv	Gi	
0.35 Vrms < OSC ≤ 1.0 Vrms	1/8	1/8	1/8	1	1	1/8	2/3
0.12 Vrms ≤ OSC ≤ 0.35 Vrms	1/8	1/8	1/8	1	1	1/8	2
40 mVrms < OSC < 0.12 Vrms	1	1	NA	NA	NA	NA	2/3
0.2 mVrms ≤ OSC < 40 mVrms	1	1	NA	NA	NA	NA	2

1 Hi-Z range appears when the impedance is higher than approx. 250 Ω and the frequency ≤ 200 MHz.

2 Lo-Z range appears when the impedance is lower than approx. 10 Ω and the frequency ≤ 200 MHz.

V/I Multiplexer

The V/I multiplexer multiplexes the V and I signals from the test head. The multiplexer is a semiconductor switch.

Control

The TRD control has two operations. One is to control the TRD amplifier circuit, the other is to send the test head ID data to the mainframe.

The TRD control receives the control data from the A6 receiver IF as serial data. It uses this data to control the TRD amplifier circuits.

The TRD control receives the test head ID data and converts the data to serial data. Then it forwards the data to the A6 receiver IF.

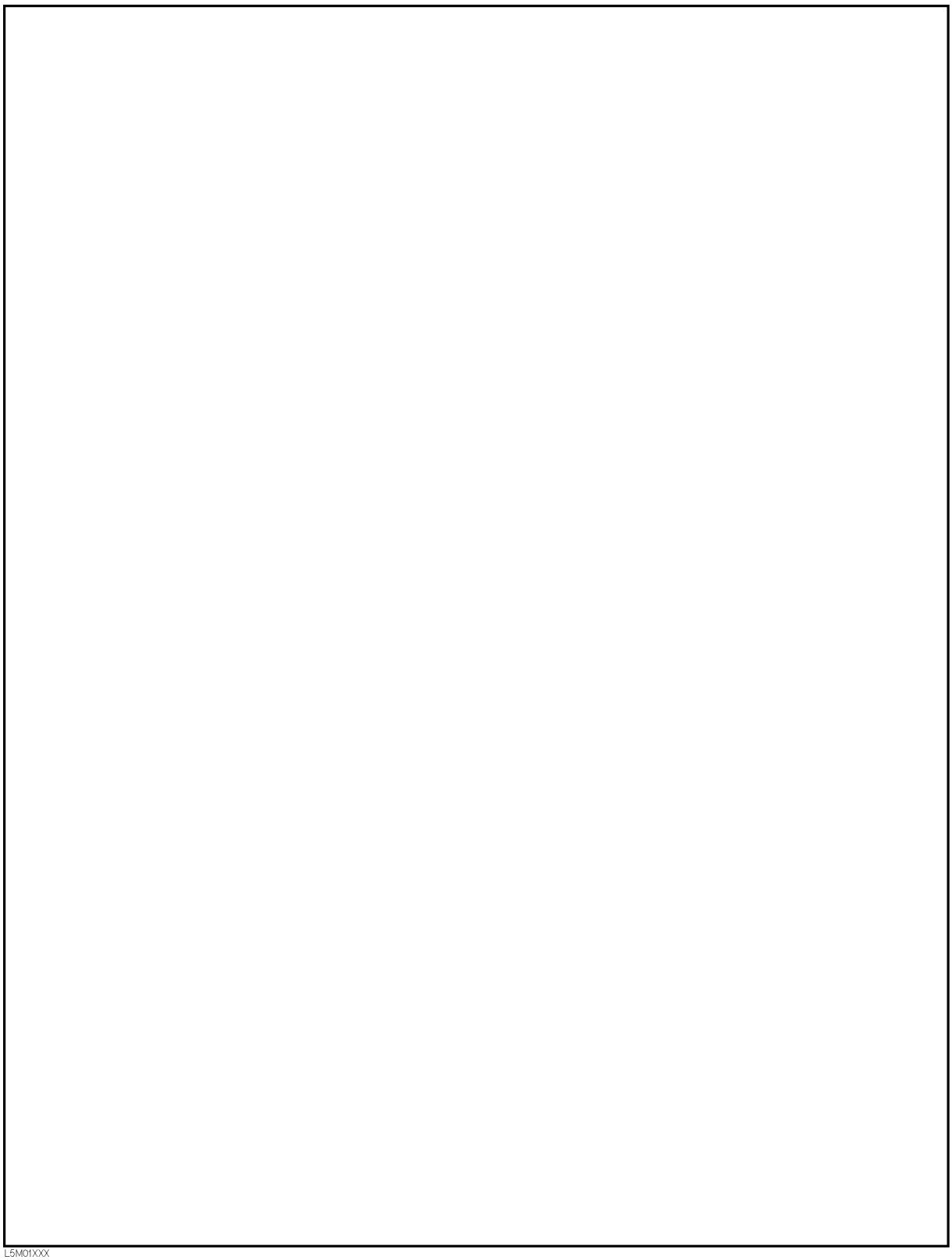


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Figure 11-10. Source Group Block Diagram

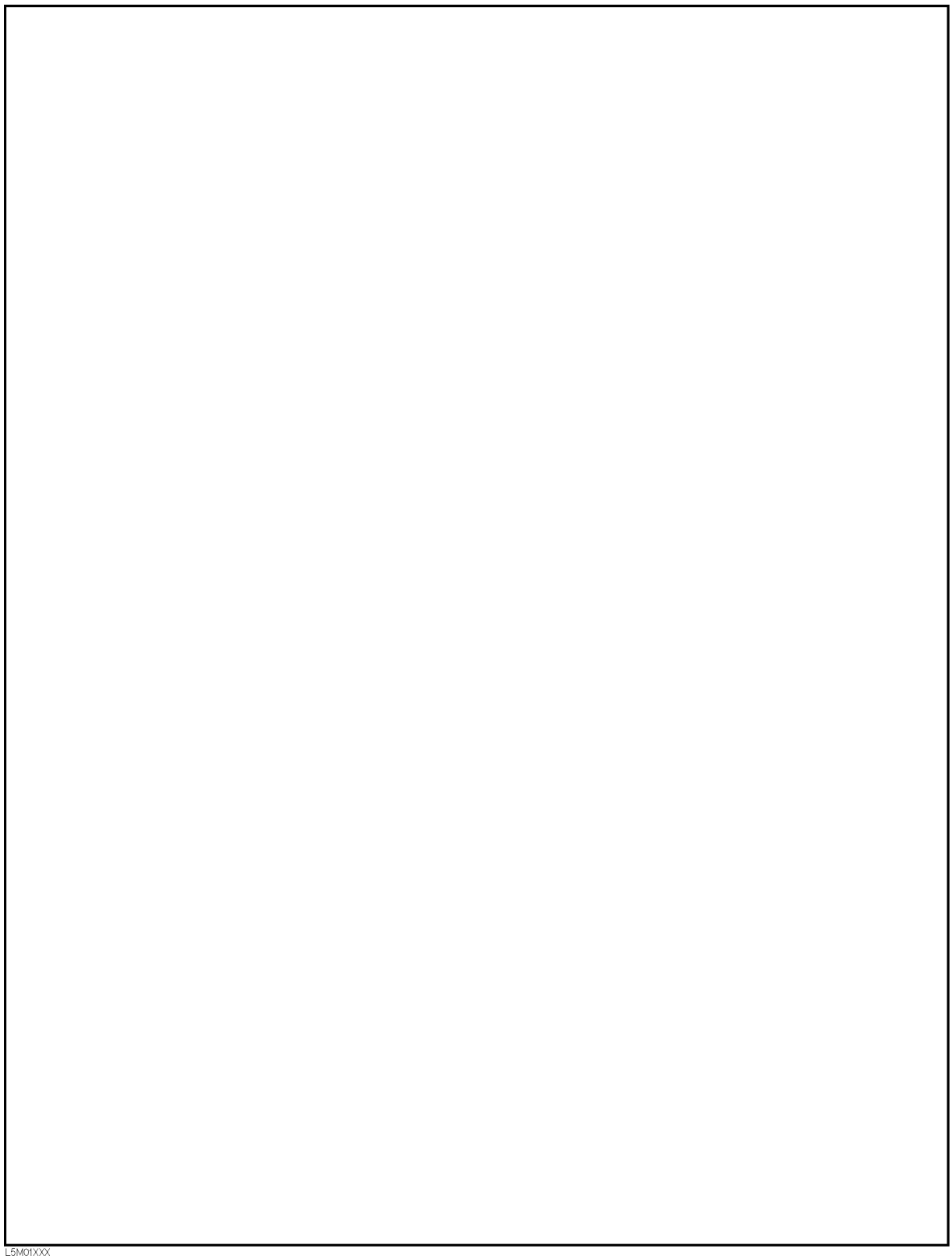

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Figure 11-11. Receiver and Transducer Groups Block Diagram

12

Replaceable Parts

INTRODUCTION

This chapter lists the analyzer's replaceable parts. How to order the parts is also described.

ORDERING INFORMATION

To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number (with a check digit), indicate the quantity required, and address the order to the nearest Hewlett-Packard office. The check digit will ensure accurate and timely processing of the order.

To order a part not listed in the replaceable parts table, include the instrument model number, the description and function of the part, and the quantity of parts required. Address the order to the nearest Hewlett-Packard office.

Direct Mail Order System

Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using this system are:

1. Direct ordering and shipment from the Hewlett-Packard Parts Center in Mountain View, California.
2. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local Hewlett-Packard office when the orders require billing and invoicing).
3. Prepaid transportation (there is a small handling charge for each order).
4. No invoices.

To provide these advantages, a check or money order must accompany each order.

Mail order forms and specific ordering information are available through your local Hewlett-Packard office, addresses and phone numbers are located at the back of this manual.

EXCHANGE ASSEMBLIES

Under the rebuilt-exchange assembly program, certain factory-repaired and tested assemblies are available on a trade-in basis. These assemblies are offered at lower cost than a new assembly while meeting all of the factory specifications required of a new assembly.

REPLACEABLE PARTS LIST

Replaceable parts tables list the following information for each part.

1 Hewlett-Packard part number.
2 Part number check digit (CD).
3 Part quantity as shown in the corresponding figure. There may or may not be more of the same part located elsewhere in the instrument.
4 Part description, using abbreviations (see Table 12-2).
5 A typical manufacturer of the part in a five-digit code (see Table 12-1).
6 The manufacturer's part number.

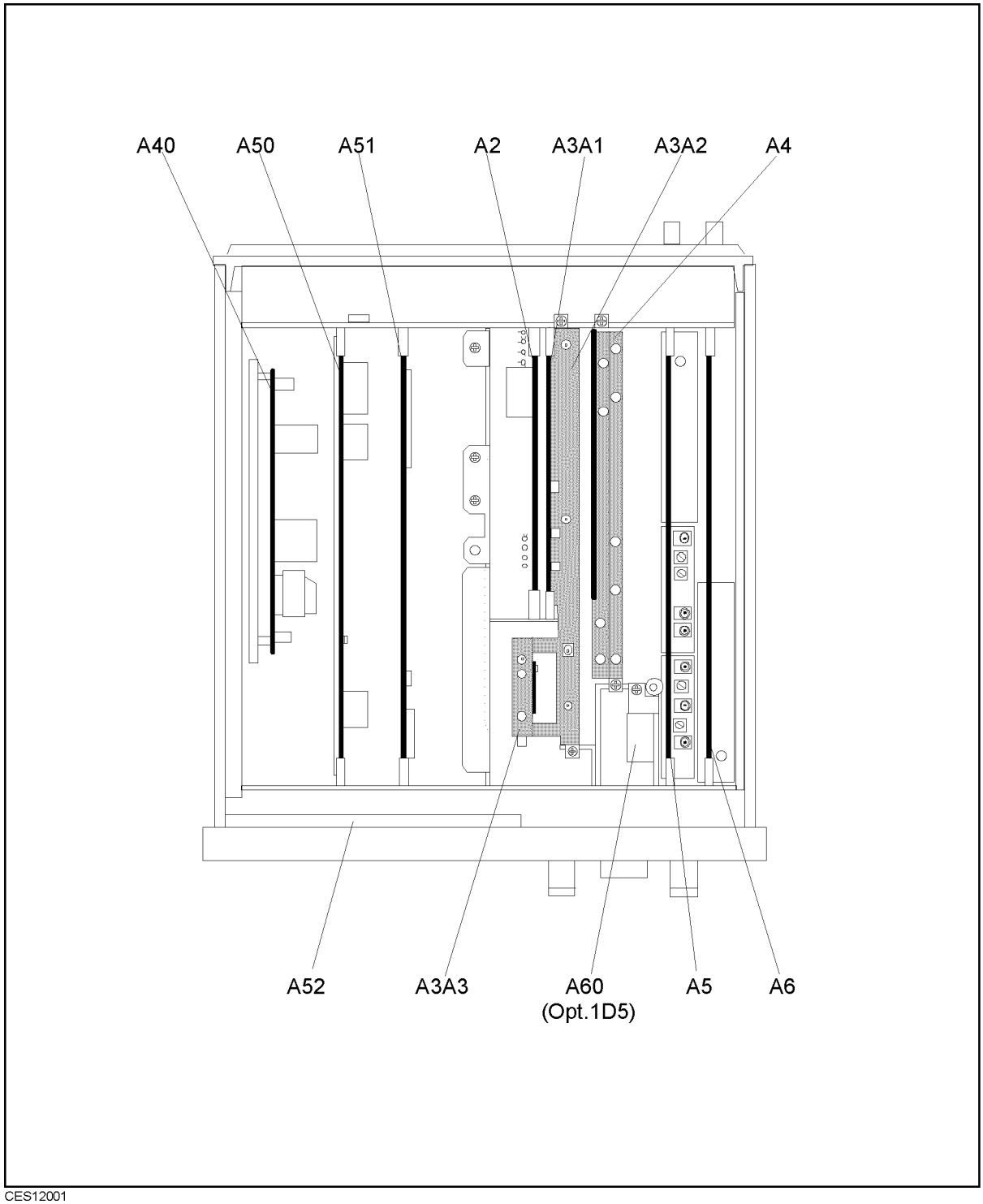
Table 12-1. Manufacturers Code List

Mfr #	Name	Location	Zipcode
00779	AMP INC	HARRISBURG PA US	17111
01125	LEWIS SCREW CO	CHICAGO IL US	60609
02788	M/A-COM INC	BURLINGTON MA US	01803
04726	3M CO	ST PAUL MN US	55144
04805	ILLINOIS TOOL WORKS INC SHAKEPROOF	ELGIN IL US	60126
06369	HIROSE ELECTRIC CO	JP	
06691	HOUSE OF METRICS LTD	SPRING VALLEY NY US	10977
08747	KITAGAWA KOGYO	TOKYO JP	
10572	XICOR INC	MILPITAS CA	
12085	SCHLEGEL CORP	ROCHESTER NY US	14692
13160	TEAC OF AMERICA INC	MONTEBELLO CA US	90640
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO CA US	94304
28520	HEYCO MOLDED PRODUCTS	KENTWORTH NJ US	07033

Table 12-2. List of Abbreviations

A	: amperes	N/C	: normally closed
A.F.C.	: automatic frequency control	NE	: neon
AMPL	: amplifier	NI PL	: nickel plate
B.F.O	: beat frequency oscillator	N/O	: normally open
BE CU	: beryllium copper	NPO	: negative positive zero (zero temperature coefficient)
BH	: binder head	NPN	: negative-positive-negative
BP	: bandpass	NRFR	: not recommended for field replacement
BRS	: brass	NSR	: not separately replaceable
BWO	: backward wave oscillator	-	: order by description
CCW	: counter-clockwise	OH	: oval head
CER	: ceramic	OX	: oxide
CMO	: cabinet mount only	P	: peak
COEF	: coefficient	PC	: printed circuit
COM	: common	p	: pico
COMP	: composition	PH BRZ	: phosphor bronze
COMPL	: complete	PHL	: Philips
CONN	: connector	PIV	: peak inverse voltage
CP	: cadmium plate	PNP	: positive-negative-positive
CRT	: cathode-ray tube	P/O	: part of
CW	: clockwise	POLY	: polystyrene
DE PC	: deposited carbon	PORC	: porcelain
DR	: drive	POS	: position(s)
ELECT	: electrolytic	POT	: potentiometer
ENCAP	: encapsulated	PP	: peak to peak
EXT	: external	PT	: point
F	: farads	PWV	: peak working voltage
f	: femto	RECT	: rectifier
FH	: flat head	RF	: radio frequency
FIL H	: fillister head	RH	: round head or right hand
FXD	: fixed	RMO	: rack mount only
G	: giga	RMS	: root-mean square
GE	: germanium	RWV	: reverse working voltage
GL	: glass	S-B	: slow-blow
GRD	: ground(ed)	SCR	: screw
H	: henries	SE	: selenium
HEX	: hexagonal	SECT	: section(s)
HG	: mercury	SEMICON	: semiconductor
HR	: hour(s)	SI	: silicon
Hz	: hertz	SIL	: silver
IF	: intermediate freq.	SL	: slide
IMPG	: impregnated	SPG	: spring
INCD	: incandescent	SPL	: special
INCL	: include(s)	SST	: stainless steel
INS	: insulation(ed)	SR	: split ring
INT	: internal	STL	: steel
k	: kilo	TA	: tantalum
LH	: left hand	TD	: time delay
LIN	: linear taper	TGL	: toggle
LK WASH	: lock washer	THD	: thread
LOG	: logarithmic taper	TI	: titanium
LPF	: low pass filter	TOL	: tolerance
m	: milli	TRIM	: trimmer
M	: meg	TWT	: traveling wave tube
MET FLM	: metal film	μ	: micro
MET OX	: metallic oxide	VAR	: variable
MFR	: manufacturer	VDCW	: dc working volts
MINAT	: miniature	W/	: with
MOM	: momentary	W	: watts
MTG	: mounting	WIV	: working inverse voltage
MY	: “mylar”	WW	: wirewound
n	: nano	W/O	: without

Top View Assemblies

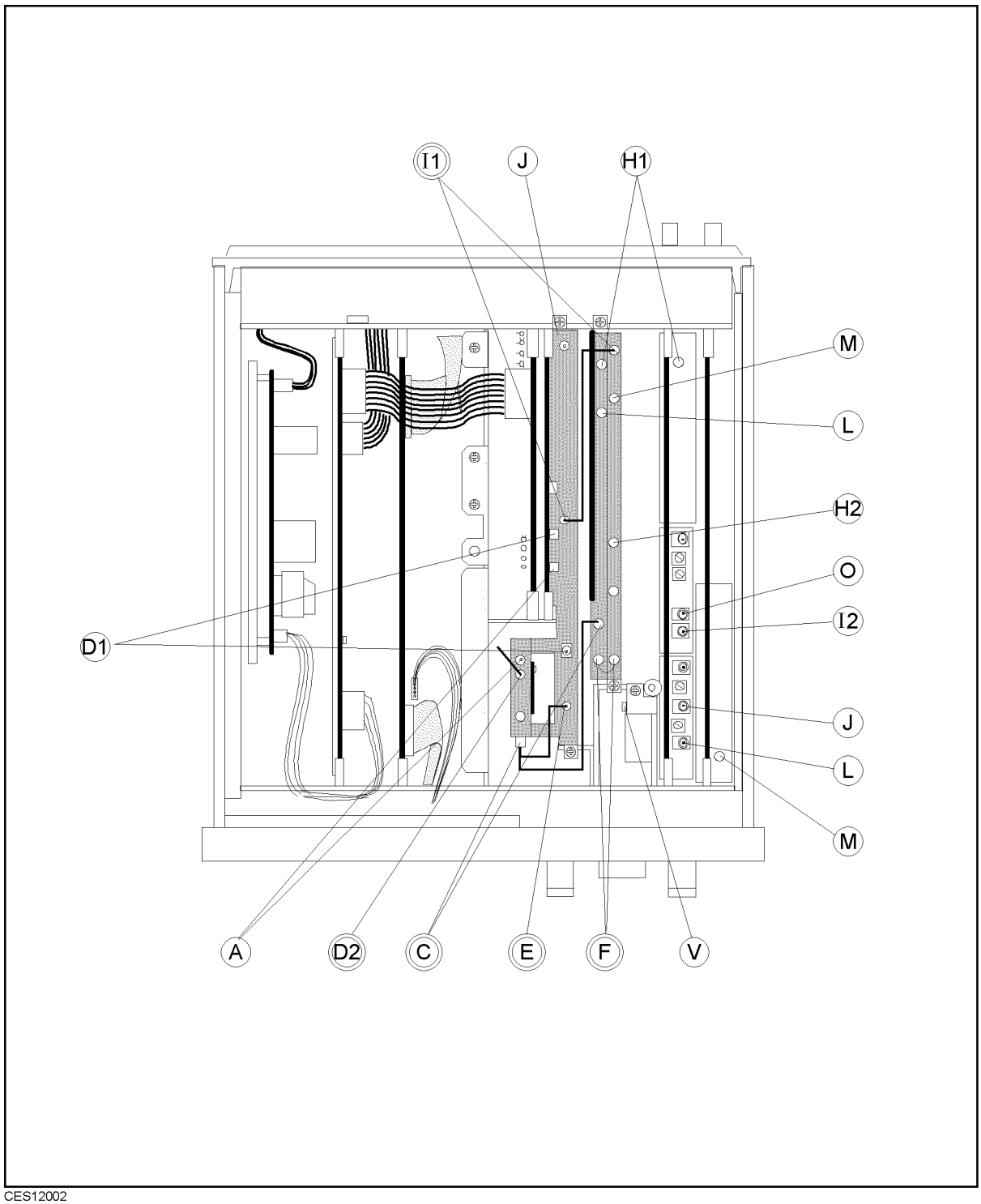


CES12001

Figure 12-1. Top View 1 (Major Assemblies)

Table 12-3. Top View 1 (Major Assemblies)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
A2	04396-66522	0	1	Post Regulator	28480	04396-66522
A3A1	04291-66503	1	1	Source Vernier	28480	04291-66503
A3A2	04396-66513	9	1	Second Lo	28480	04396-66513
A3A2	04396-69513	5		Second Lo (rebuilt-exchange)	28480	04396-69513
A3A3	5086-7620	1	1	Source	28480	5086-7620
A3A3	5086-6620			Source (rebuilt-exchange)	28480	5086-6620
A4	04396-61004	3	1	First LO/Receiver RF	28480	04396-61004
A4	04396-69004	9		First Lo/Receiver RF (rebuilt-exchange)	28480	04396-69004
A5	04396-66505	9	1	Synthesizer	28480	04396-66505
A5	04396-69505	5		Synthesizer (rebuilt-exchange)	28480	04396-69505
A6	04291-65506	4	1	Receiver IF	28480	04291-65506
A6	04291-69506	0	1	Receiver IF (rebuilt-exchange)	28480	04291-69506
A30	04396-66530	0	1	Front Keyboard	28480	04396-66530
A40	0950-3246	7	1	Preregulator	28480	0956-3246
A50	E4970-66550	7	1	DC-DC Converter	28480	E4970-66550
A51	E4970-66552	9	1	GSP	28480	E4970-66552
A52	2090-0574	6	1	LCD	28480	2090-0574
A60	04396-61060	1	1	Freq Ref (opt. 1D5)	28480	04396-61060



CES12002

Figure 12-2. Top View 2 (RF Flexible and RF Semi-rigid Cables)

Note Alphabetic designators in Figure 12-2 show the cable markers.

Table 12-4. Top View 2 (RF Flexible and RF Semi-rigid Cables)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Connection	
A	04396-61621	0	1	RF Cable "A"	A3A1	A3A3
D_1	04396-61622	1	1	RF Cable "D"	A3A2	A3A3
H_1	04396-61623	2	1	RF Cable "H"	A4	A5
H_2	04291-61615	6	1	RF Cable "H"	A4	Front "R"
I_2	04396-61634	5	1	RF Cable "I"	A4	Rear, EXT REF
J	04396-61625	4	1	RF Cable "J"	A3A2	A5
L	04396-61624	3	1	RF Cable "L"	A4	A5
M	04396-61626	5	1	RF Cable "M"	A4	A6
O	04396-61633	4	1	RF Cable "O"	A5	Rear, INT REF
V	04396-61636	7	1	RF Cable "V" (Opt.1D5)	A60	Rear, REF OVEN
C	04396-61603	8	1	RF Semi-Rigid Cable "C"	A3A3	A4
D_2	04291-61616	7	1	RF Semi-Rigid Cable "D"	A3A3	A7
E	04396-61605	0	1	RF Semi-Rigid Cable "E"	A3A2	A3A3
F	04396-61606	1	1	RF Semi-Rigid Cable "F"	A4	A4
I_1	04396-61609	4	1	RF Semi-Rigid Cable "I"	A3A2	A4

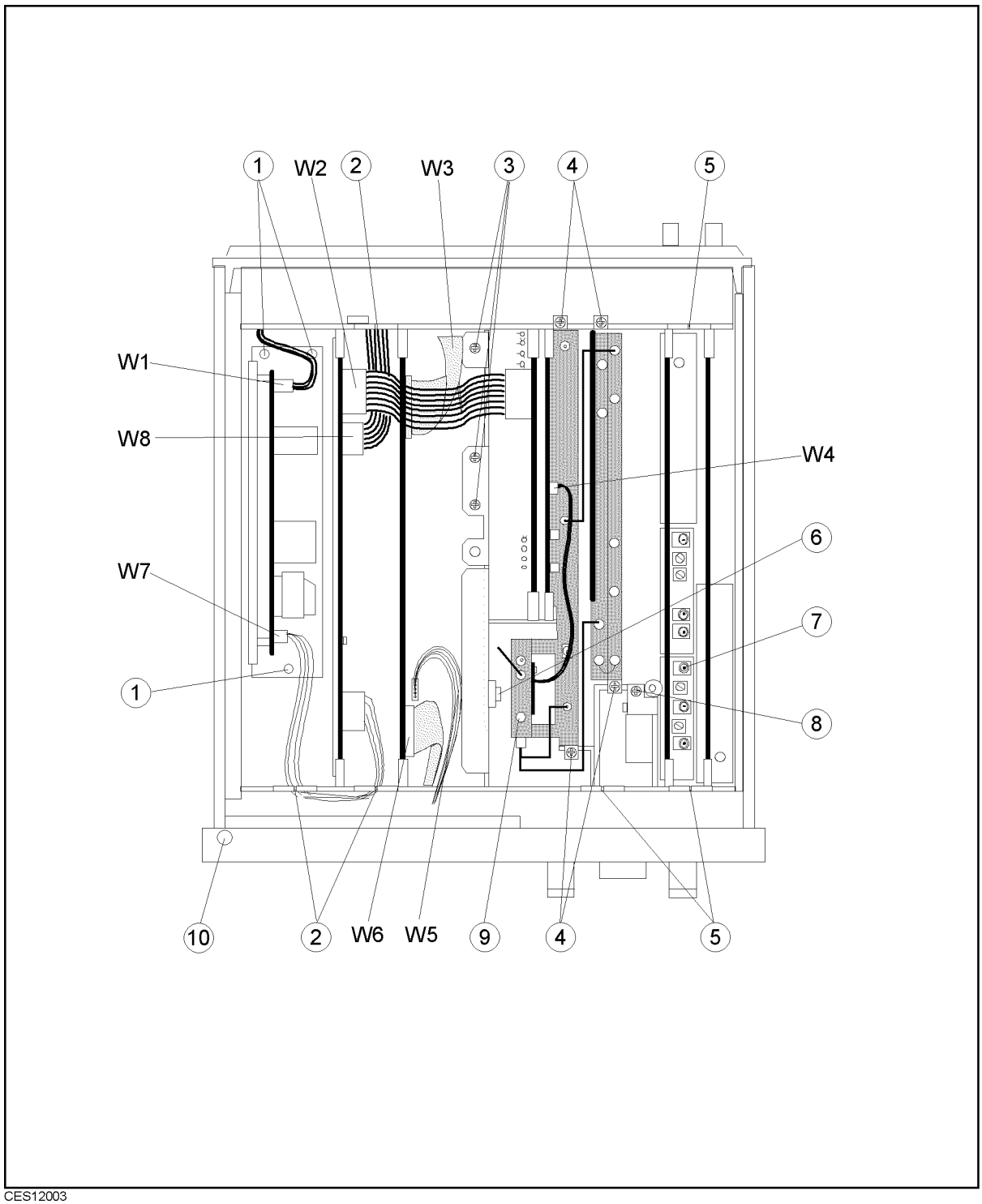


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Figure 12-3. Top View 3 (Wires and Misc. Parts)

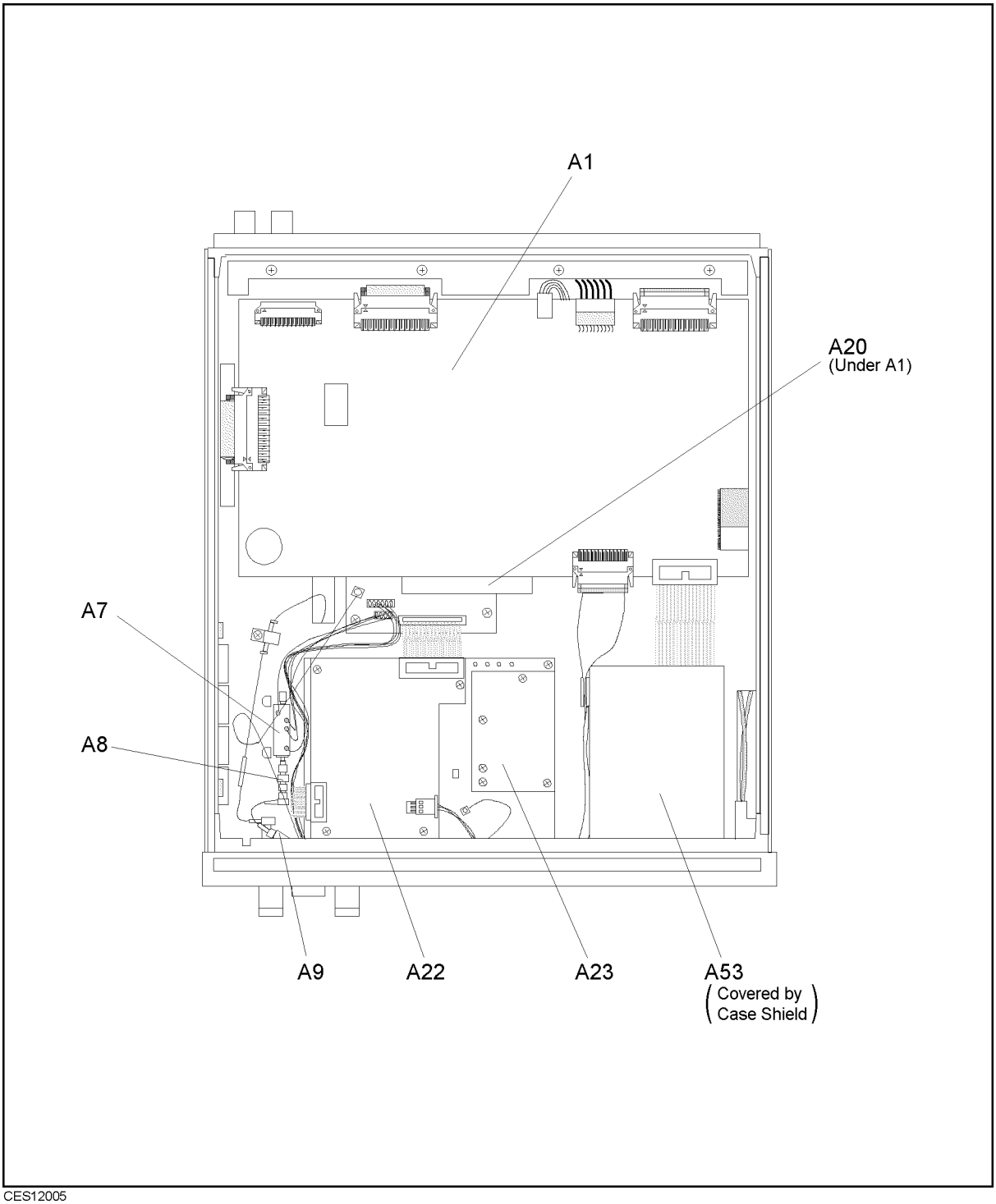
Table 12-5. Top View 3 (Wires)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Connection	
W2	04396-61674	3	1	Wire	A2	A40
	04291-61605	4	1	Wire (Opt. 001)	A2	A40, A22
W3	04396-61707	3	1	Flat Cable	A1	A51
W4	04396-61673	2	1	Wire	A3A1	A3A3
W5	04396-61709	5	1	Wire	A51	LCD
W6	E4970-61651	9	1	Flat Cable	A51	LCD
W7	04396-61709	5	1	Wire	A40	A50
W8	04396-61671	0	1	Wire	A1	A50

Table 12-6. Top View 3 (Misc. Parts)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	0515-1719	3	3	Screw M4 (for A40)	28480	0515-1719
2	1400-2198	2	3	Saddle Edge	28480	1400-2198
3	0515-1550	0	3	Screw M3 (for A2)	28480	0515-1550
4	0515-2079	0	4	Screw M4 (for A3A2, A4)	28480	0515-2079
5	1400-1048	9	3	Saddle Edge	28480	1400-1048
6	1400-1334	6	1	Clamp Cable	08747	K-104G
7	See Table 12-3		1	Termination (Part of A5)		
8	0515-1550	0	1	Screw M3 (for A60)	28480	0515-1550
9	1810-0118	1	2	Termination SMA	28480	1810-0118
10	0515-0889	6	8	Screw M3.5 (for front frame)	28480	0515-0889

Bottom View Assemblies

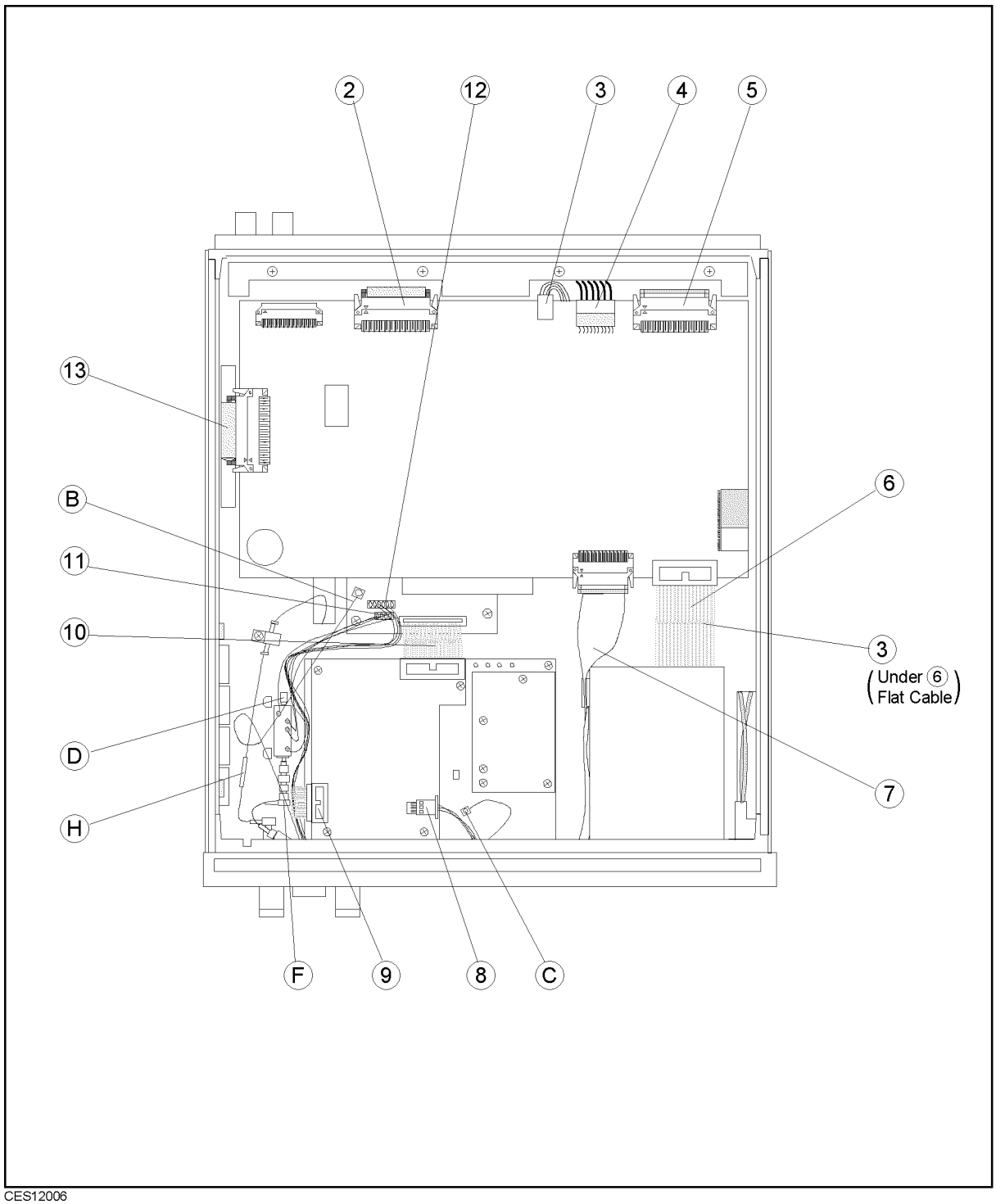


CES12005

Figure 12-4. Bottom View 1 (Major Assemblies)

Table 12-7. Bottom View 1 (Major Assemblies)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
A1	E4970-66501	8	1	CPU	28480	E4970-66501
A7	0955-0664	7	1	Output ATT	28480	0955-0664
A8	0955-0701	3	1	Output 3 dB ATT	28480	0955-0701
A9	0955-0701	3	1	Input 3 dB ATT	28480	0955-0701
A20	04291-66520	2	1	Motherboard	28480	04291-66520
A22	04291-66522	4	1	DC Bias 1/2 (Opt. 001)	28480	04291-66522
A23	04291-66523	5	1	DC Bias 2/2 (Opt. 001)	28480	04291-66523
A53	0950-3208	1	1	FDD	28480	0950-3208



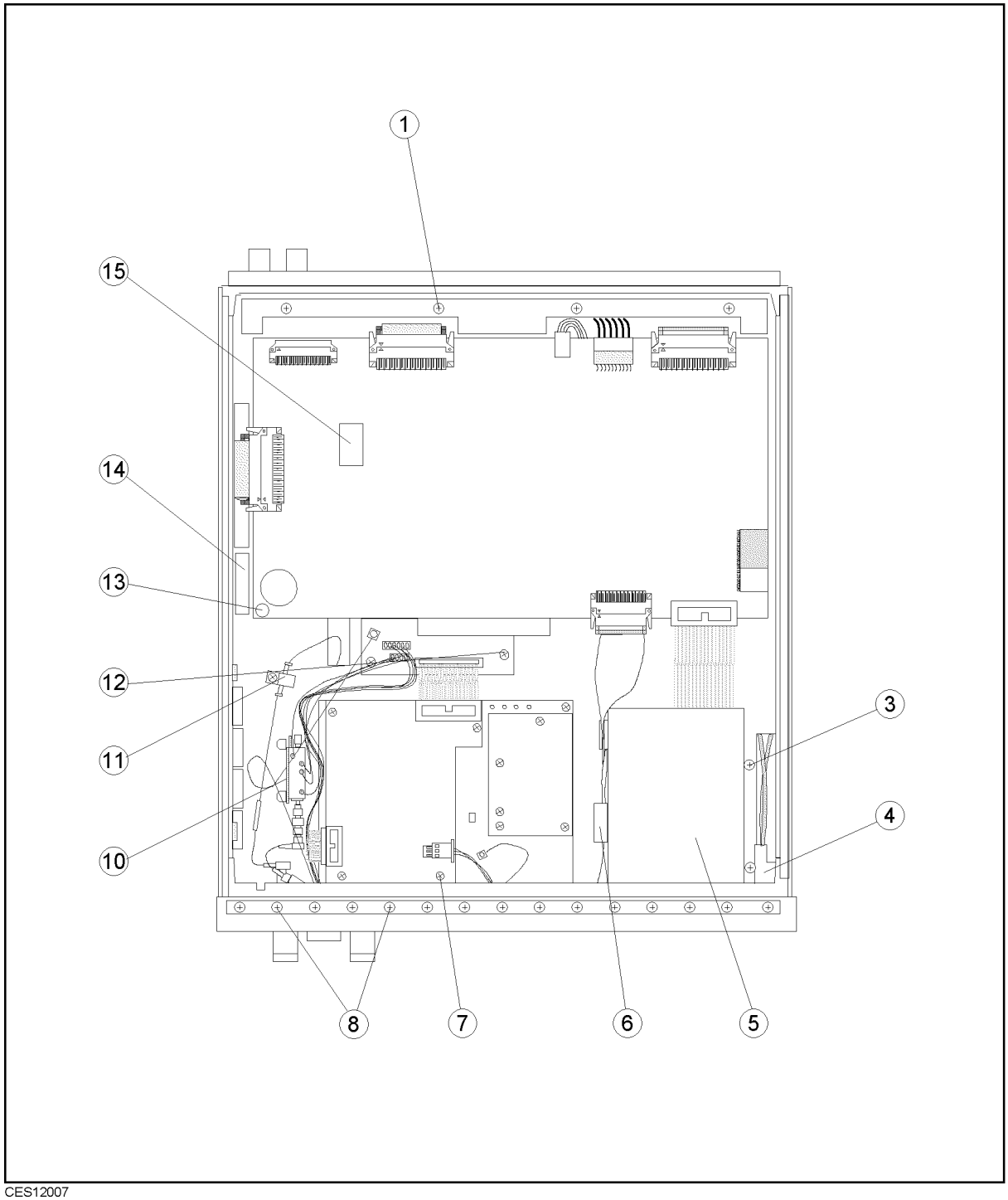
CES12006

Figure 12-5. Bottom View 2 (RF Cables, and Wires)

Note Alphabetic designators in Figure 12-5 show the cable markers.

Table 12-8. Bottom View 2 (RF Semi-rigid Cables, and Wires)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Connection	
B	04291-61006	9		Front Conn. and Cable Assy (STD)	Front	A20
	04291-61001	4		Front Conn. and Cable Assy (Opt.001)	Front	A20, A23
C	04291-61001	4		Front Conn. and Cable Assy (Opt.001)	Front	A20, A23
D	See Table 12-4			RF Cable "D"	A3A3	A7
F	04291-61612	3	1	RF Cable "F"	Front "S"	A8
H	See Table 12-4			RF Cable "H"	Front "R"	A4
2	04396-61662	9	1	Flat Cable	A1	A31
3	04396-61672	1	1	Wire	A1	A53
4	See Table 12-5			Wire	A1	A40
5	See Table 12-5			Flat Cable	A1	A51
6	04396-61651	6	1	Flat Cable	A1	A53
7	04396-61662	9	1	Flat Cable	A1	A30
8	See Table 12-5			Wire (Opt.001)	A40	A2, A22
9	04291-61608	7	1	Flat Cable (Opt.001)	A22	A23
10	04291-61609	8	1	Flat Cable (Opt.001)	A20	A22
11	04291-61604	3	1	Wire	A7	A20
12	04291-61006	9		Front Conn. and Cable Assy (STD)	Front	A20
	04291-61001	4		Front Conn. and Cable Assy (Opt.001)	Front	A20, A23
13	04396-61661	8	1	Flat Cable	A1	A20



CES12007

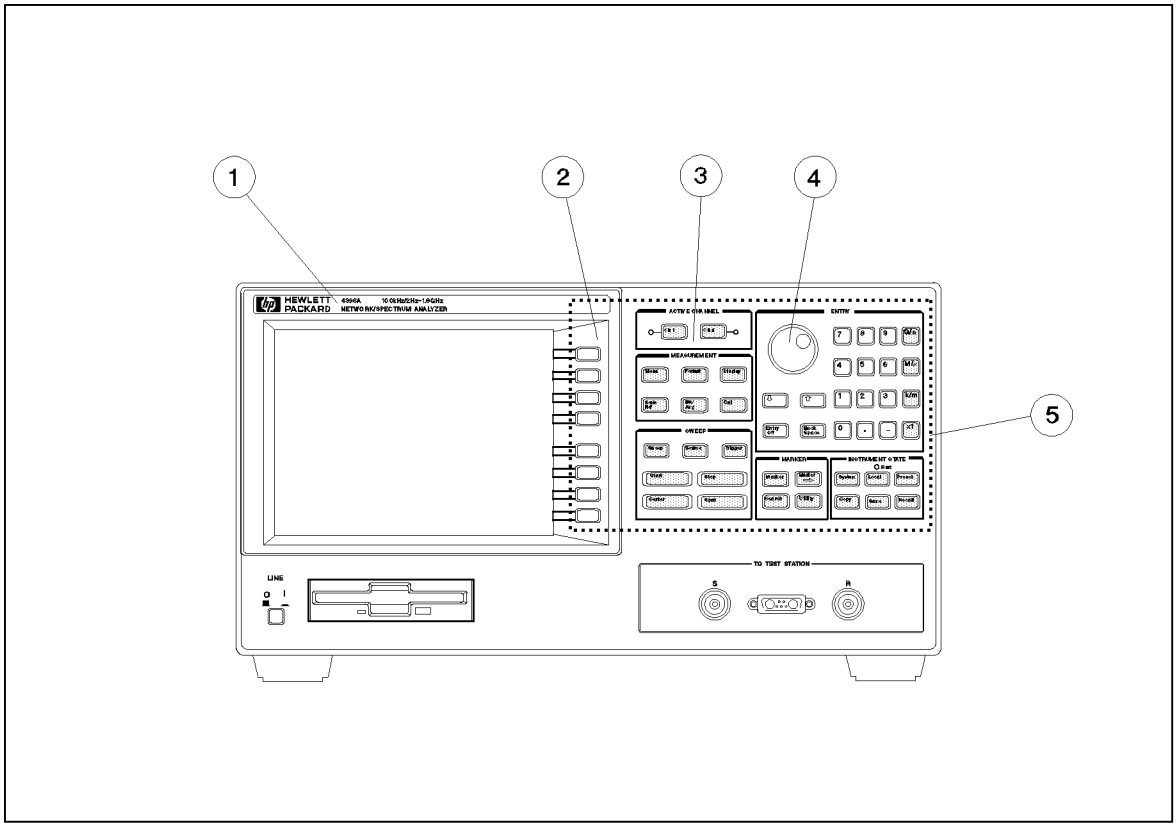
Figure 12-6. Bottom View 3 (Miscellaneous Parts)

Table 12-9. Bottom View 3 (Miscellaneous Parts)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	0515-1719	3	3	Screw M4	28480	0515-1719
3	0535-0031	2	4	Nut M3	28480	0535-0031
4	04396-61701	7	1	PS Switch Assy	28480	04396-61701
	5041-0564	4	1	Key Cap	28480	5041-0564
	04396-01274	3	1	Switch Holder	28480	04396-01274
	0515-0999	9	2	Screw M2.5	28480	0515-0999
5	04396-01275	4	1	Holder	28480	04396-01205
	0515-0914	8	4	Screw M3 (for Holder)	28480	0515-0914
	04396-25004	7	1	Sponge (for Holder)	28480	04395-25004
6	1400-0611	0	1	Clamp, Flat Cable	04726	3484-1000
7	0515-1550	0	9	Screw M3 (for A22,A23)	28480	0515-1550
8	0515-0889	6	6	Screw M3.5	28480	0515-0889
10	04291-01231	6	1	Holder	28480	04291-01231
	0515-1550	0	4	Screw M3 (for Holder)	28480	0515-1550
11	1400-0015	8	1	Clamp, Cable	28480	1400-0015
	0515-2079	0	1	Screw M4	28480	0515-2079
12	0515-1550	0	14	Screw M3 (for A20)	28480	0515-1550
13	0515-1550	0	13	Screw M3 (for A1)	28480	0515-1550
14	04291-01291	8	1	Shield	28480	04291-01291
	0515-0914	8	5	Screw M3 (for Chassis)	28480	0515-0914
	1400-1334	6	2	Clamp Cable	28480	1400-1334
	0403-0179	0	2	Bumper Foot	28480	0403-0719
15	1818-5146	1	1	EEPROM[1]	10572	X28C64P-20

1 Included in A1

Front Assembly Parts

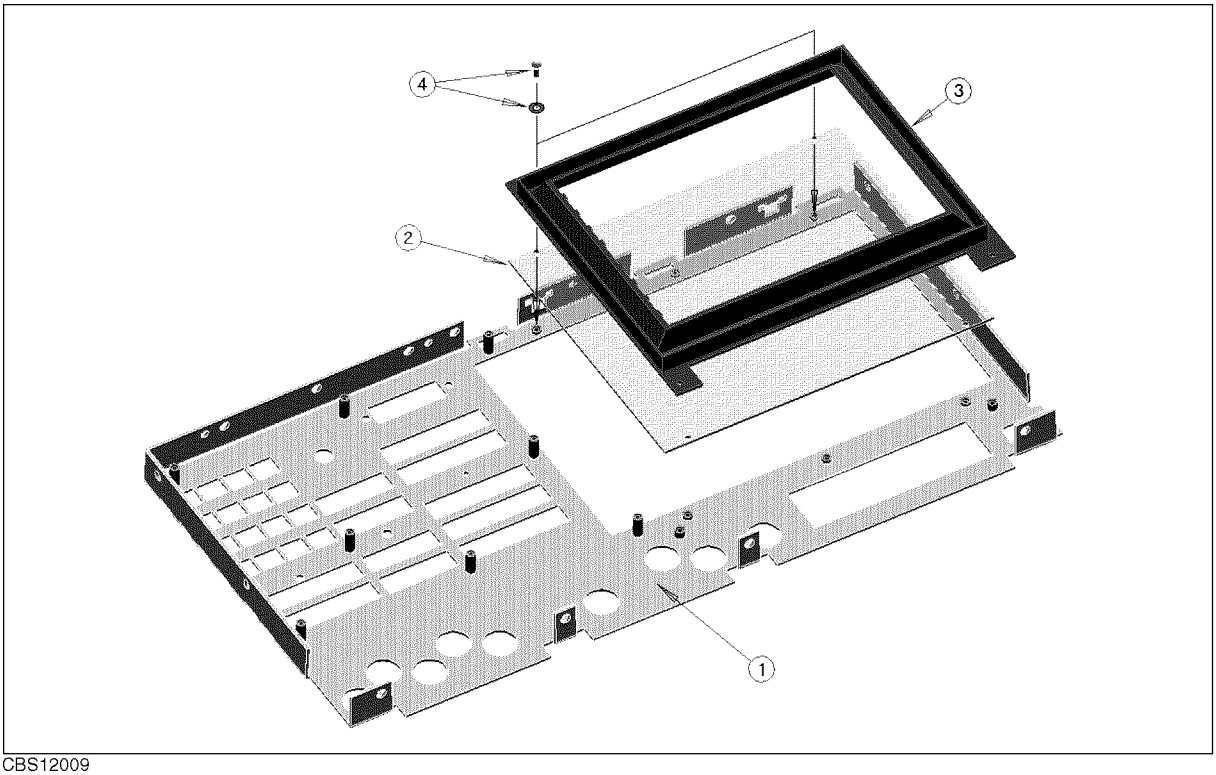


C6S12001

Figure 12-7. Front Assembly Parts 1/5 (Outside)

Table 12-10. Front Assembly Parts 1/5 (Outside)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	04291-87121	3	1	Label	28480	04291-87121
2	04396-40051	6	1	Bezel	28480	04396-40051
3	04291-00221	2	1	Panel Front	28480	04291-00221
	04191-08000	0	1	Spring between Front Panel and Sub Panel	28480	04191-08000
4	5182-7522	6	1	Knob	28480	5182-7522
5	04396-25051	4	1	Rubber Key	28480	04396-25051

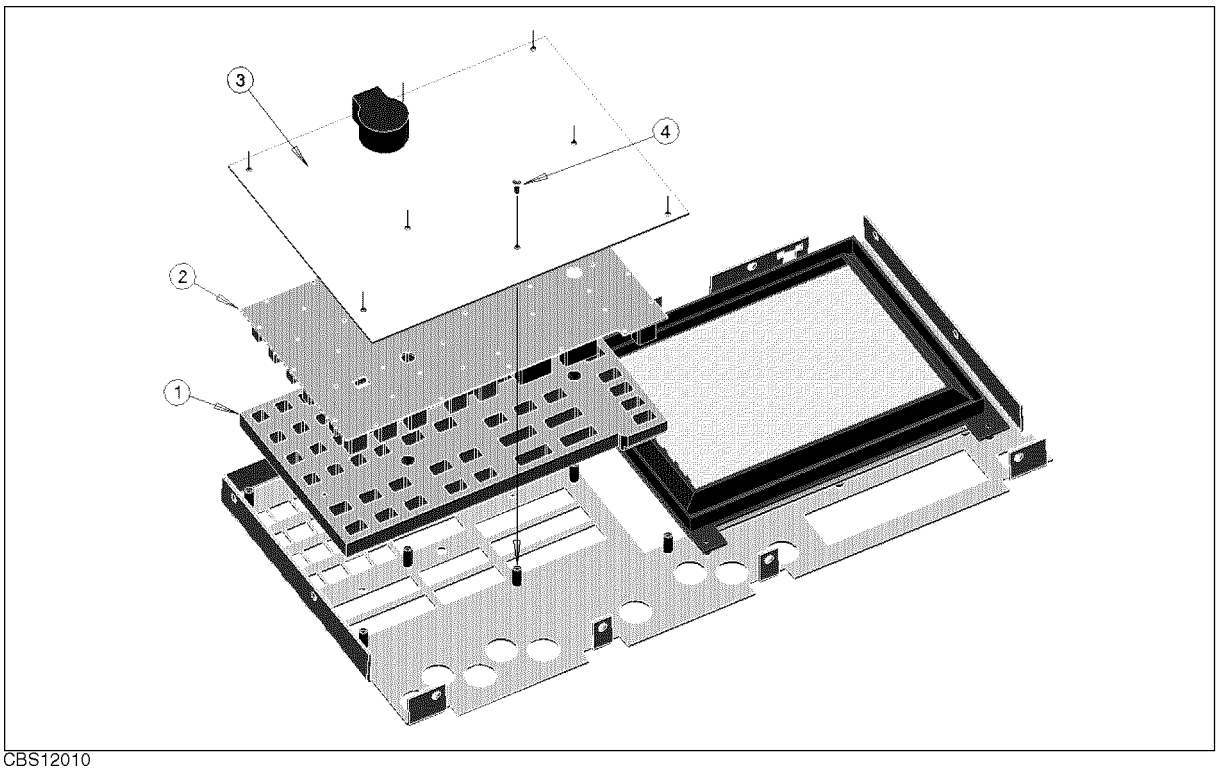


CBS12009

Figure 12-8. Front Assembly Parts 2/5 (Inside)

Table 12-11. Front Assembly Parts 2/5 (Inside)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	04291-00222	9	1	PANEL SUB	28480	04396-00272
2	E4970-25001	7	1	FILTER	28480	E4970-25001
3	04396-40071	0	1	BEZEL BACK	28480	04396-40071
4	0515-1550	0	2	SCR M3-L 8 P-H	28480	0515-1550
	3050-0891	7	2	WASHER M3	28480	3050-0891

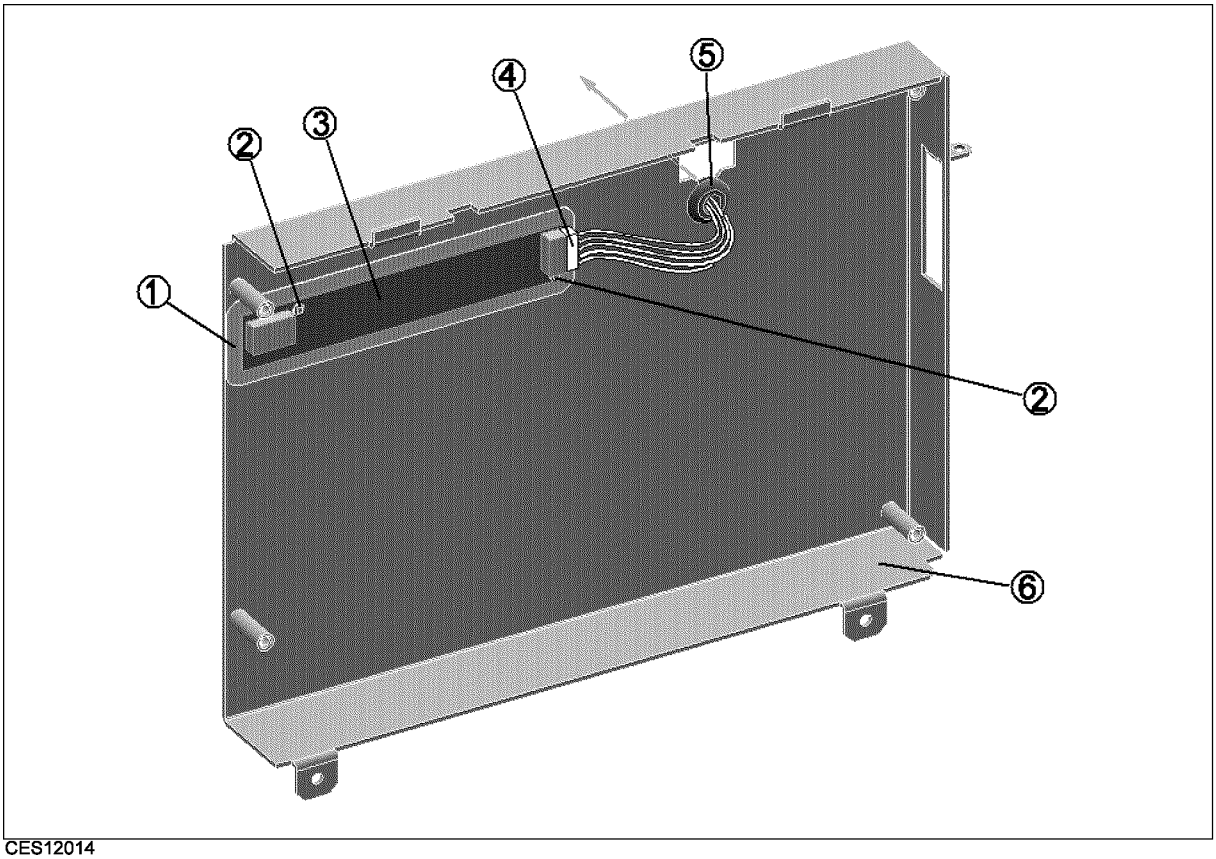


CBS12010

Figure 12-9. Front Assembly Parts 3/5 (Inside)

Table 12-12. Front Assembly Parts 3/5 (Inside)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	04396-40003	8	1	GUIDE	28480	04396-40003
2	04396-25051	4	1	KEYPAD RUBBER	28480	04396-25051
3	04396-66530	0	1	A30 Front Keyboard	28480	04396-66530
4	0515-1550	0	8	SCR M3-L 8 P-H	28480	0515-1550

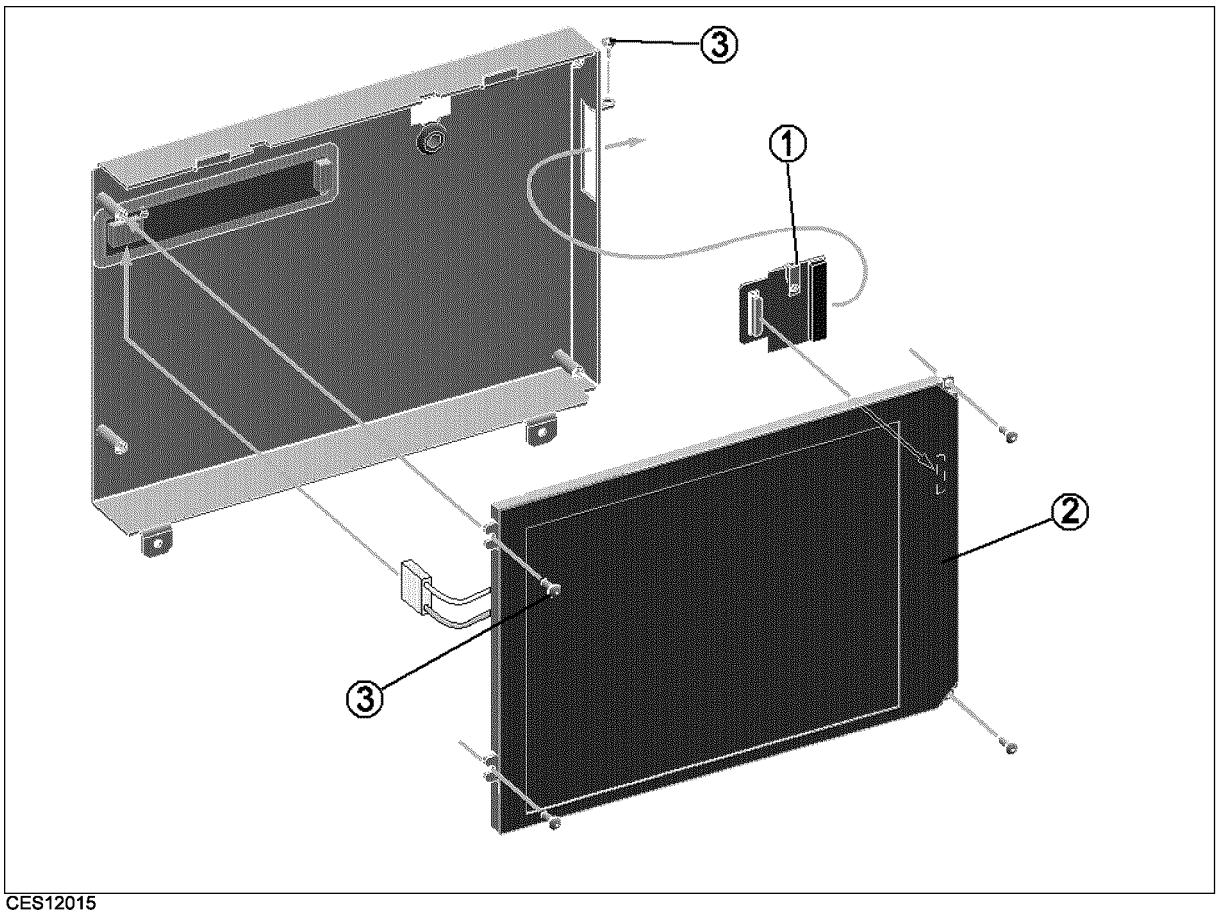


CES12014

Figure 12-10. Front Assembly Parts 4/5 (Inside)

Table 12-13. Front Assembly Parts 4/5 (Inside)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	E4970-25002	8	1	INSULATOR	28480	E4970-25002
2	0515-0977	3	2	SCR-MACH M2X0.4	28480	0515-0977
3	0950-2924	6	1	A54 Inverter	28480	0950-2924
4	04396-61709	5	1	CABLE ASSY	28480	04396-61709
5	0400-0010	2	1	GROMET	28480	0400-0010
6	E4970-04002	4	1	LCD COVER	28480	E4970-04002



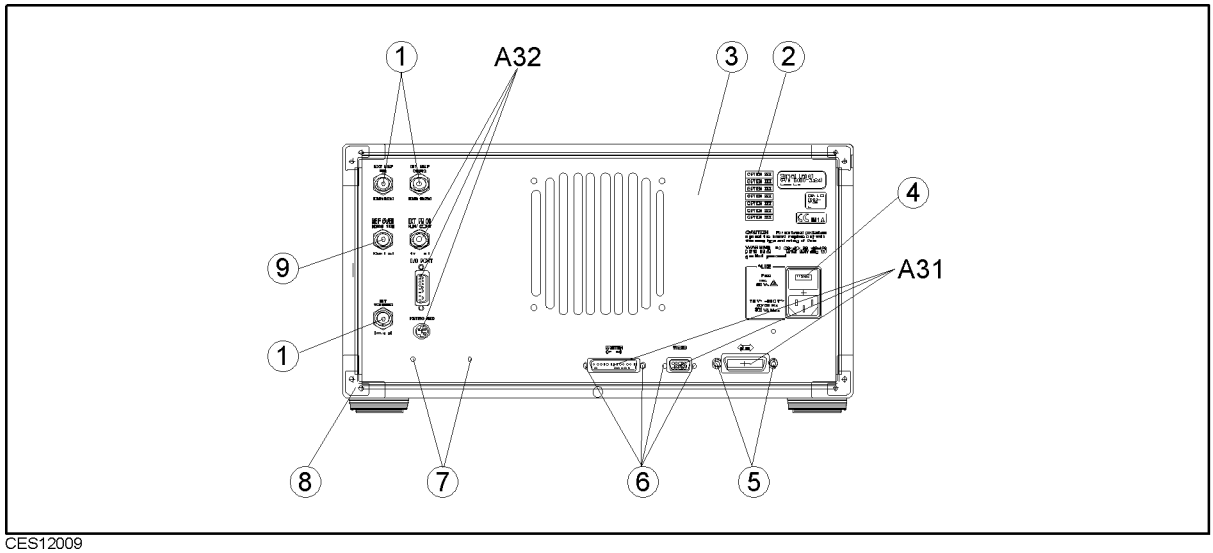
CES12015

Figure 12-11. Front Assembly Parts 5/5 (Inside)

Table 12-14. Front Assembly Parts 5/5 (Inside)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	E4970-66539	2	1	Mini-Board	28480	E4970-66539
2	2090-0574	8	1	A52 LCD	28480	2090-0574
	04396-25071	8	1	GASKET	28480	04396-25071
3	0515-1550	0	5	SCR M3-L 8 P-H	28480	0515-1550

Rear Assembly Parts

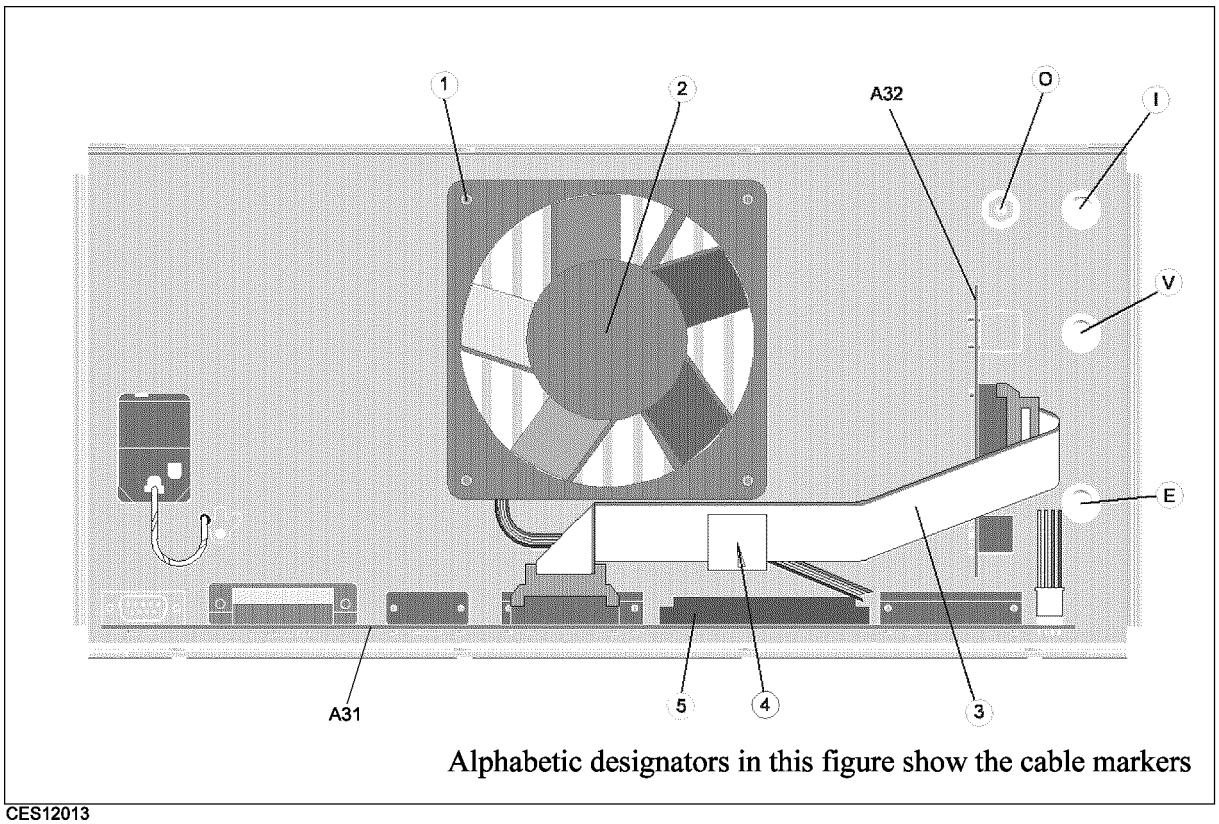


CES12009

Figure 12-12. Rear Assembly Parts 1 (Outside)

Table 12-15. Rear Assembly Parts 1 (Outside)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	1250-0252	6	3	Connector BNC	28480	1250-0252
	2190-0102	8	3	Washer (for Connector)	78189	1922-01
	2950-0035	8	3	Nut (for Connector)	28480	2950-0035
2	7120-0381	3	1	Label Opt.001	28480	7120-0381
	7120-0382	4	1	Label Opt.002	28480	7120-0382
	5080-3923	7	1	Label Opt.1D5	28480	5080-3923
3	04291-00203	0	1	Panel Rear	28480	04291-00203
4	1252-6951	8	1	AC Inlet	28480	1252-6951
	2110-0917	5	1	Fuse	28480	2110-0030
	2110-1134	0	1	Fuse Holder	28480	2110-1134
5	0380-0644	4	2	Standoff	28480	0380-0644
	2190-0577	9	1	Washer (for Standoff)	28480	2190-0577
6	1251-7812	0	4	Jackscrew	28480	1251-7812
7	0515-1550	0	2	Screw M3	28480	0515-1550
8	5041-8821	2	4	Stand Off	28520	5041-8821
	0515-1232	5	4	Screw M3	28480	0515-1232
9	6960-0041	1	1	Plug Hole (Std.)	28520	2643(BLACK)
	1250-0252	6	1	Connector BNC (Opt.1D5)	28480	1250-0252
	2190-0102	8	1	Washer (for Connector)	78189	1922-01
	2950-0035	8	1	Nut (for Connector)	28480	2950-0035



CES12013

Figure 12-13. Rear Assembly Parts 2 (Inside)

Table 12-16. Rear Assembly Parts 2 (Inside)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
A31	E4970-66536	9	1	I/O Connector	28480	E4970-66536
A32	E4970-66532	5	1	IBASIC I/F	28480	E4970-66532
	3050-1546	1	1	Spacer for BNC (A32 - rear panel)	28480	3050-1546
	2190-0054	9	1	Washer (for BNC)	78189	1924-12
	2950-0054	1	1	Nut (for BNC)	28480	2950-0054
	1251-7812	0	2	Screw (for I/O Port)	28480	1251-7812
1	3050-0893	9	4	Washer Flat	28480	3050-0893
	2190-0586	2	4	Washer Spring	06691	A2WASPSR 0158
	0515-1598	6	4	Screw M4	28480	0515-1598
2	04396-61001	0	1	Fan Assembly	28480	04396-61001
3	04396-61706	2	1	Flat Cable	28480	04396-61706
4	1400-1334	6	1	Clamp Cable	28480	1400-1334
5	See Table 12-8			Flat Cable (A32 to A20)		
E	04396-61635	6	1	RF Cable “E” (to A20)	28480	04396-61635
I	See Table 12-4			RF Cable “I”		
O	See Table 12-4			RF Cable “O”		
V	See Table 12-4			RF Cable “V” (Opt.1D5)		

Miscellaneous Parts

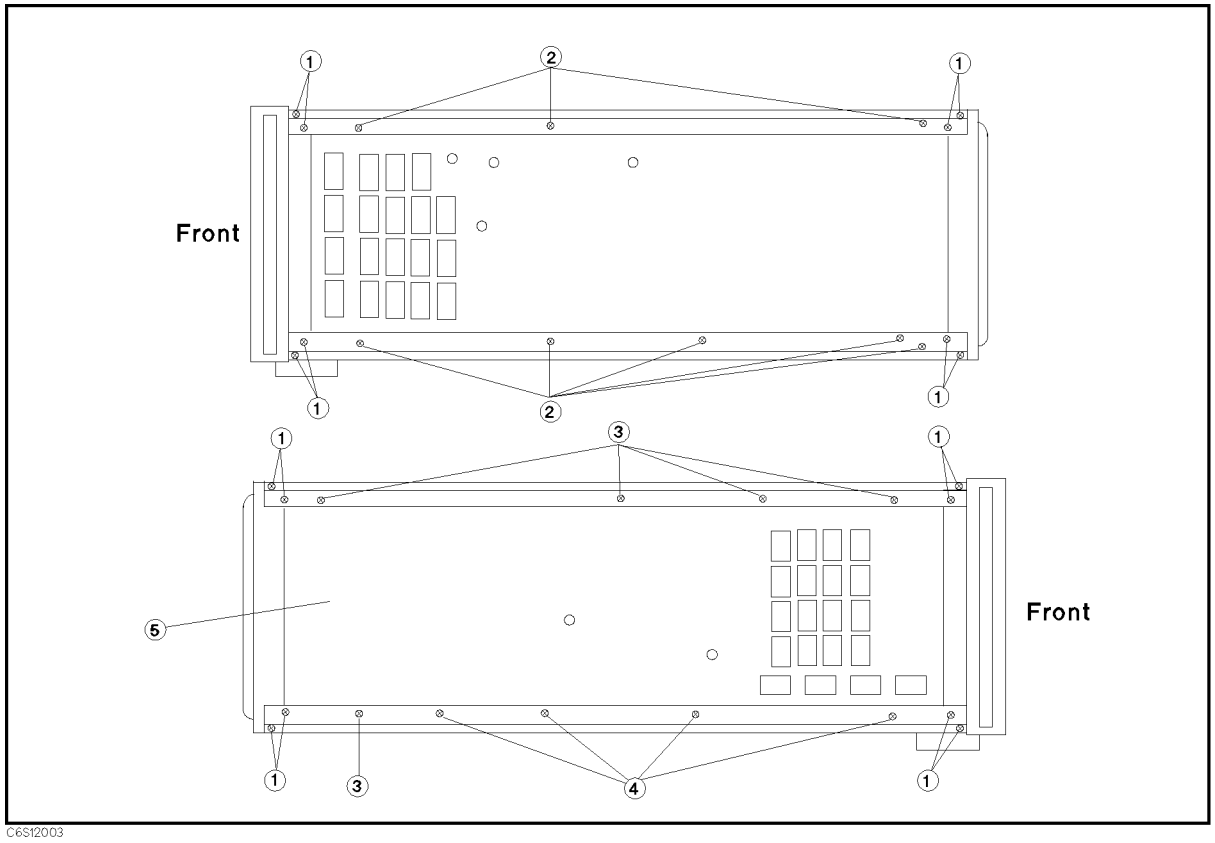


Figure 12-14. Miscellaneous Parts 1 (Side Viwes)

Table 12-17. Miscellaneous Parts 1 (Side Viwes)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	0515-1668	1	16	Screw	28480	0515-1668
2	0515-1719	3	8	Screw M4	28480	0515-1719
3	0515-2079	0	5	Screw M4	28480	0515-2079
4	0515-1718	2	4	Screw M4	28480	0515-1718
5	04291-60001	2	1	Chassis	28480	04291-60001

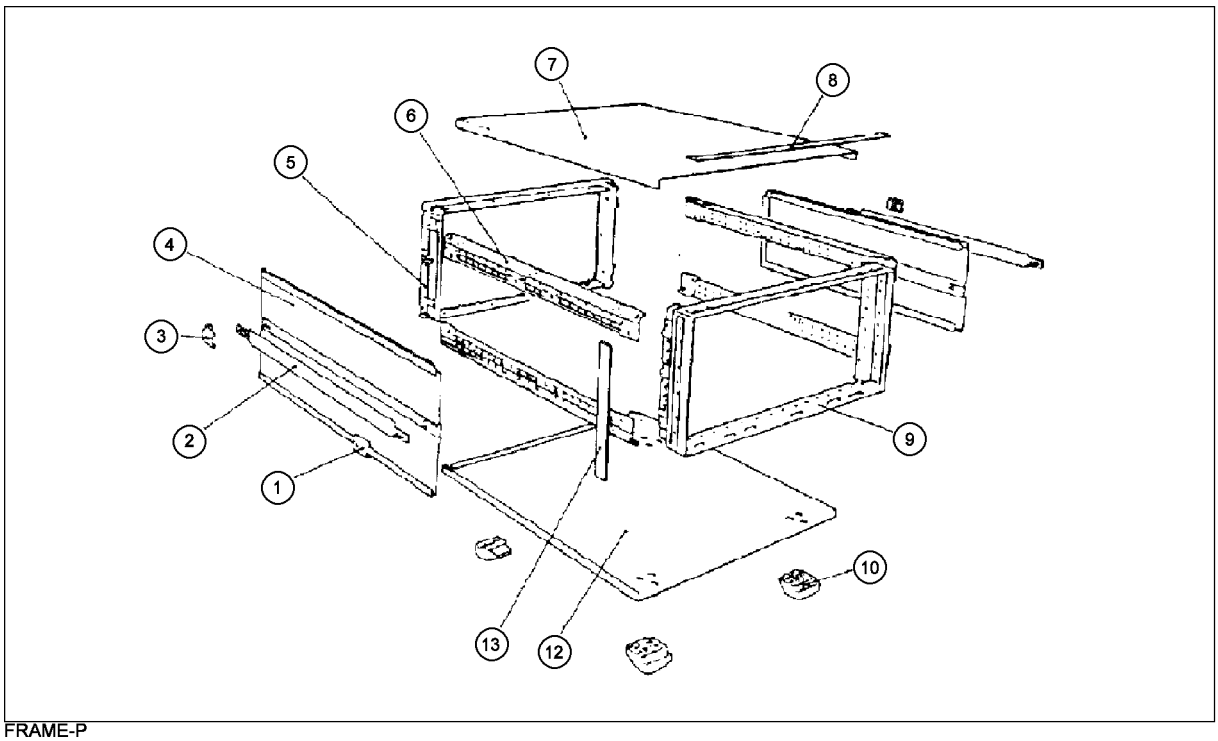


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Figure 12-15. Miscellaneous Parts 2 (Chassis)

Table 12-18. Miscellaneous Parts 2 (Chassis)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	5041-9186	4	2	Cap-Front	28480	5041-9186
	0515-1132	4	2	Screw M5	28480	0515-1132
2	5063-9210	1	2	Strap Handle	28480	5063-9210
3	5041-9187	5	2	Cap-Rear	28480	5041-9187
	0515-1132	4	2	Screw M5	28480	0515-1132
4	5002-3989	1	2	Side Cover	28480	5002-3989
5	5021-5808	7	1	Rear Frame	28480	5021-5808
6	5021-5837	2	4	Corner Strut	28480	5021-5837
7	5002-1047	8	1	Top Cover	28480	5002-1047
8	5041-9176	2	1	Top Trim	28480	5041-9176
9	5022-1190	4	1	Front Frame	28480	5022-1190
10	5041-9167	1	4	Foot	28480	5041-9167
	1460-1345	5	2	Tilt Stand	28480	1460-1345
12	5002-1088	7	1	Bottom Cover	28480	5002-1088
13	5041-9173	9	2	Side Trim	28480	5041-9173

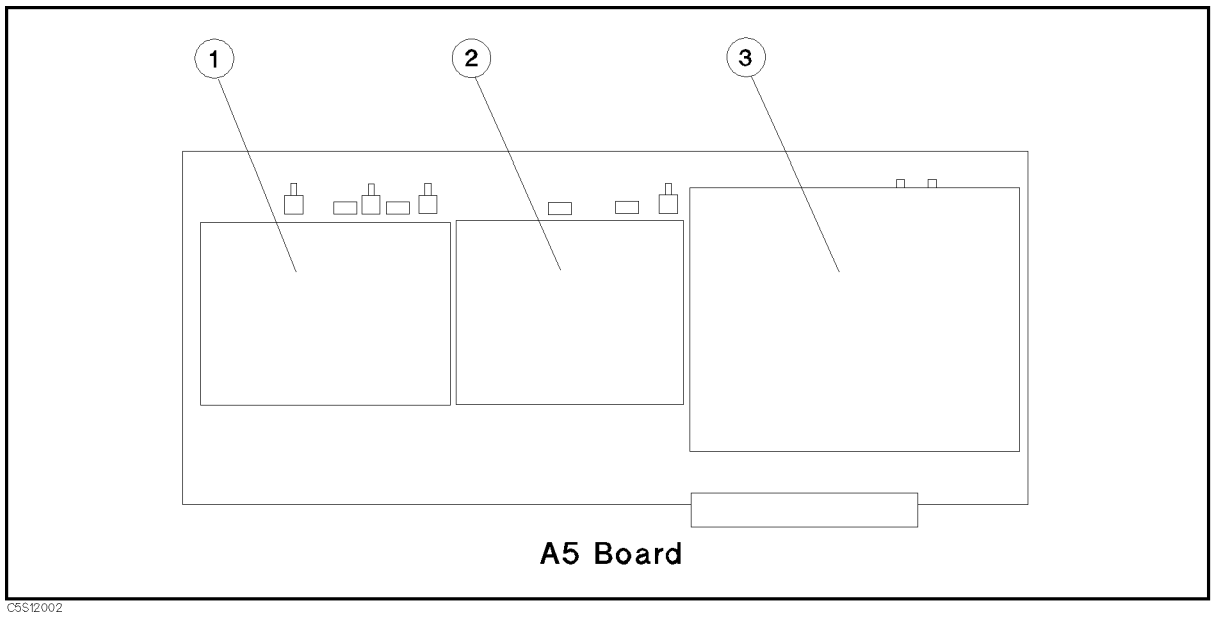

Figure 12-16. Miscellaneous Parts 3 (On A5)

Table 12-19. Miscellaneous Parts 3 (On A5)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	04396-00651	8	1	Case Shield Component Side	28480	04396-00651
	04396-00652	9	1	Case Shield Component Side	28480	04396-00652
	0515-0914	8	4	Screw M3	28480	0515-0914
2	04396-00653	0	1	Case Shield Component Side	28480	04396-00653
	04396-00654	1	1	Case Shield Component Side	28480	04396-00654
	0515-0914	8	7	Screw M3	28480	0515-0914
3	04396-00655	2	1	Case Shield Component Side	28480	04396-00655
	04396-00656	3	1	Case Shield Component Side	28480	04396-00656
	0515-0914	8	4	Screw M3	28480	0515-0914

Parts listed in Table 12-19 are included in A5.

Table 12-20. Miscellaneous Parts 4 (Other Shields)

HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
04396-00611	0	1	Plate Shield Top	28480	04396-00611
8160-0694	6	3 cm	Gasket (for Plate Shield)	12085	UC300275
8160-0781	2	3 cm	Gasket (for Plate Shield)	12085	UC300227
0515-0913	7	3	Screw M4 (for Plate Shield)	28480	0515-0913
0515-0914	8	12	Screw M3 (for Plate Shield)	28480	0515-0914
04396-00632	5	1	Case Shield (A3A1 Circuit Side)	28480	04396-00632
0515-1005	0	4	Screw M3 (for Case Shield)	28480	0515-1005
8160-0512	7	23cm	Gasket in A3A2 Case Shield	28480	8160-0512
0515-1550	0	4	Screw M3 (for A3A2)	28480	0515-1550
04291-00625	0	1	Case Shield (A6 Component Side)[1]	28480	04291-00625
04291-00626	1	1	Case Shield (A6 Circuit Side)[1]	28480	04291-00626
0515-0914	8	5	Screw M3 (for Case Shield)[1]	28480	0515-0914
04291-00621	6	1	Case Shield (A23 Component Side)[2]	28480	04291-00621
0515-0914	8	5	Screw M3 (for Case Shield)[1]	28480	0515-0914
04291-00623	8	1	Case Shield (A23 Circuit Side)[2]	28480	04291-00623
0515-1550	0	4	Screw M3	28480	0515-1550

1 Included in A6

2 Included in A23

Table 12-21. Miscellaneous Parts 5 (Accessories)

HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
04291-18000	2	1	Program Disk Set	28480	04291-18000
See Figure B-2			Power Cable		
1250-1859	1	1	Adapter BNC to BNC[1]	28480	1250-1859
C3757-60401	-	1	Mini DIN Keyboard	-	-
			Calibration Kit		
04191-85302	7	1	0 S Termination	28480	04191-85302
04191-85300	5	1	0 Ω Termination	28480	04191-85302
04291-65006[2]	2	1	50 Ω Termination	28480	04291-65006
04291-60042	1	1	Low-loss Capacitor	28480	04291-60042
04291-60041	0	1	Carrying Case	28480	04291-60041
			Service Software		
04291-65003	4		Adjustment Program[3]	28480	04291-65003
			Documentation		
04291-90020	8	1	Operating Manual	28480	04291-90020
04291-90027	5	1	Programming Manual	28480	04291-90027
E2083-90005	0	1	HP IBASIC Handbook	28480	E2083-90005
04291-90111	8	1	Service Manual[4]	28480	04291-90111

1 Option 1D5 only

2 *Calibration Kit Contents List* must be filled out in the 50 Ω replacement.

3 Not furnished

4 Option 0BW only

Test Station and Test Head Parts

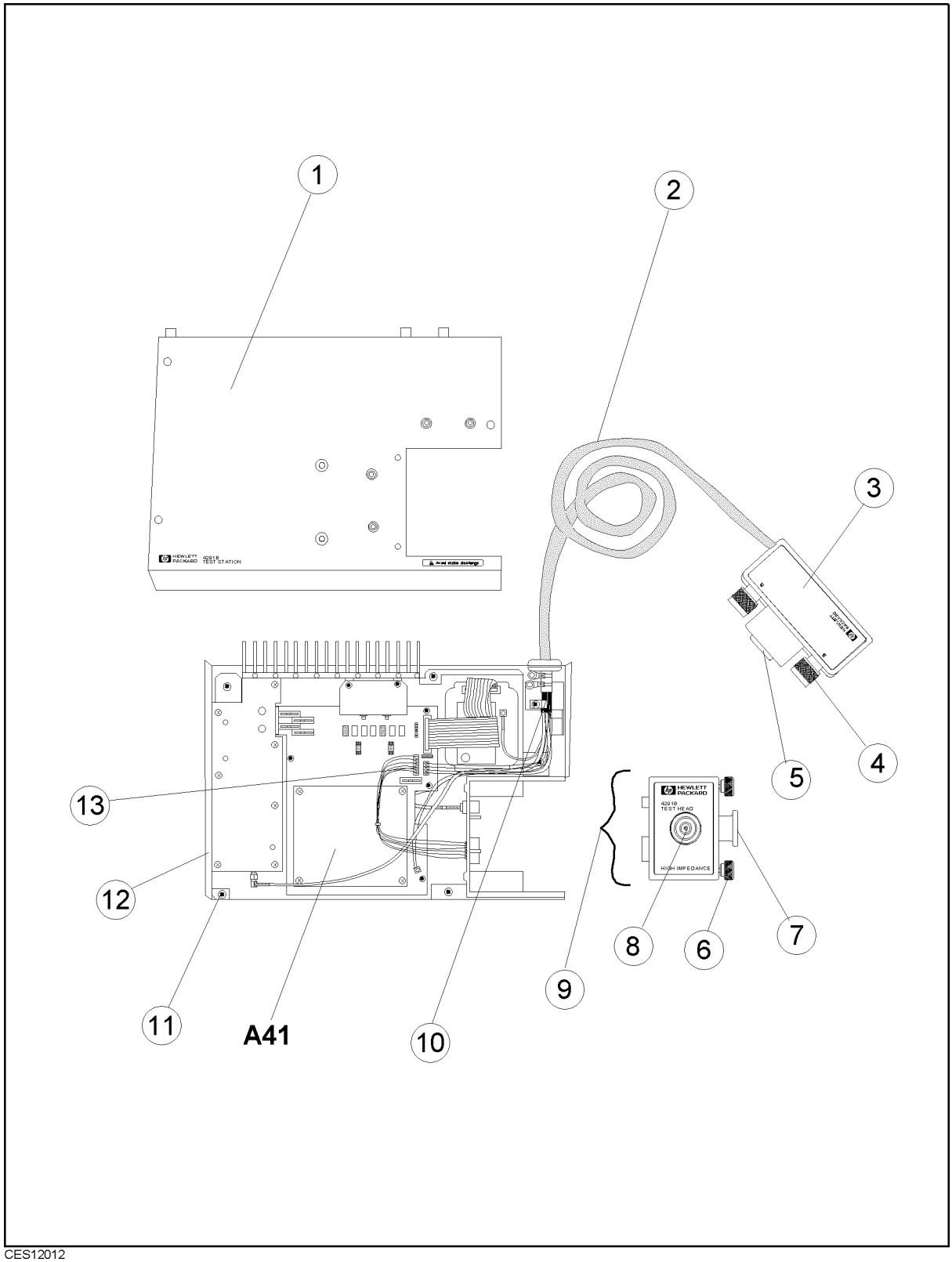

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Figure 12-17. Test Station and Test Head Parts

Table 12-22. Test Station and Test Head Parts

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
A41	04291-65041	0	1	TRD Amp	28480	04291-65041
A41	04291-69041	8	1	TRD Amp (rebuilt-exchange)	28480	04291-69041
1	04291-04051	4	1	Cover Top	28480	04291-04051
	0515-0914	8	10	Screw M3 (for cover top)	28480	0515-0914
2	04291-61061	6	1	Cable Assembly	28480	04291-61061
3	04291-20071	2	1	Case Top	28480	04291-20071
	04291-20072	3	1	Case Bottom	28480	04291-20072
	04291-87151	9	1	Label	28480	04291-87151
	0515-1718	2	2	Screw M4 (for case)	28480	0515-1718
	6960-0081	9	1	Plug Hole	28480	6960-0081
4	1250-2468	0	2	Connector N-SMA		
	0515-0907	9	8	Screw M3L8 (for connector)		
5	04291-61061	6		Cable Assembly	28480	04291-61061
	1460-2369	5	2	Spring	28480	1460-2369
6[1]	04291-24068	5	2	Knob	28480	04291-24068
	04291-25062	1	2	Insulator (for Knob)	28480	04291-25062
	2190-0014	1	2	Washer LK (for Knob)	28480	2190-0014
	2190-0586	1	2	Washer FL (for Knob)	28480	2190-0586
7[1]	04291-01282	7	1	Angle	28480	04291-01282
	0515-0914	8	2	Screw M3 (for angle)	28480	0515-0914
8[1]	1250-0820	4	1	Connector APC7	28480	1250-0820
	85020-20001	7	1	Center conductor collet (6-slot)	28480	85050-20001
9[2]	04291-60141	1	1	High Z Test Head	28480	04291-60141
	04291-60142	2	1	Low Z Test Head (Opt.012)	28480	04291-60142
10	1400-0015	8	1	Clamp Cable	28480	1400-0015
	0515-2079	0	1	Screw M4	28480	0515-2079
11	0515-2079	0	5	Screw M4 (for A41)	28480	0515-2079
12	04291-04056	9	1	Cover Bottom	28480	04291-04056
	0403-0424	8	4	Foot		
13[3]	04291-61041	2	1	Cable Assembly	28480	04291-61041

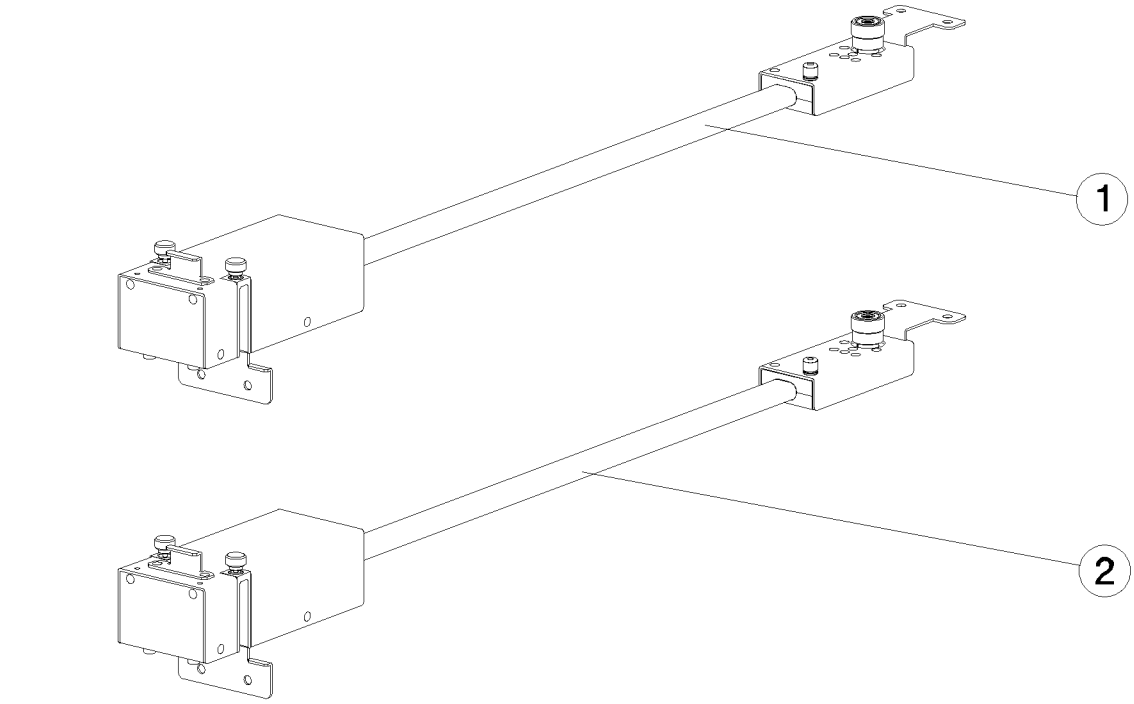
1 Part of test head, designated 9

2 Cover Bottom must be replaced from a defective head, see Chapter 13 for details.

3 Part of A41

High Temperature Test Head Parts (Option 013 and 014)

Table 12-23. High Temperature Test Head Parts

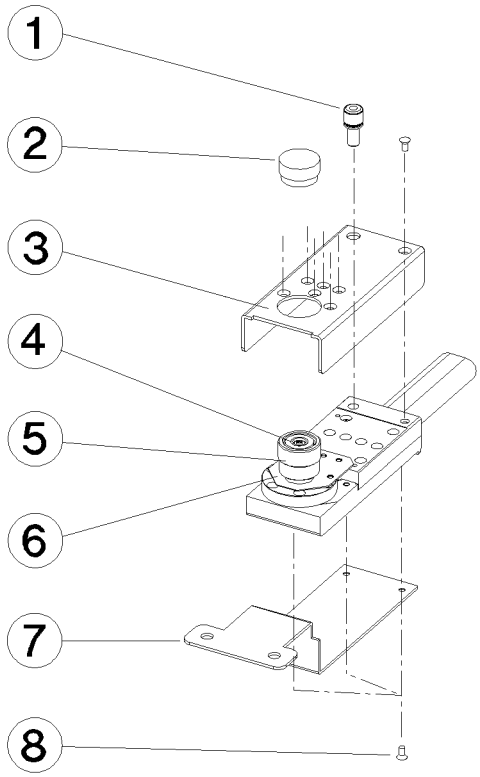


Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	04291-60143[1 2]	3	1	High-Temp. High-Z Test Head (Opt.013)	28480	04291-60143
2	04291-60144[1 2]	4	1	High-Temp. Low-Z Test Head (Opt.014)	28480	04291-60144

1 HP internal-only part number.

2 Bottom cover must be replaced from a defective unit in order to maintain serial number. See Chapter 13 for details.

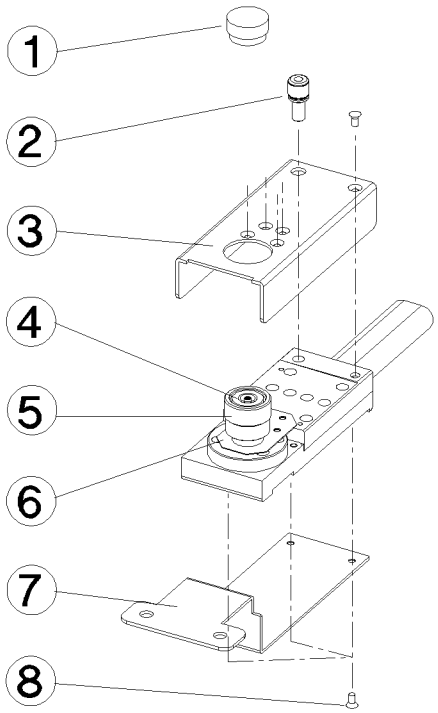
Table 12-24. High Temp. Test Heads Parts (Fixture Side, Option 013)



C6S12006

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	1510-0130	1	1	B-POST	28480	1510-0130
2	16190-25011	3	1	CAP, APC-7®	28480	16190-25011
3	04291-04005	8	1	TOP COVER	28480	04291-04005
4	1250-0820	4	1	CMPNT-RF CONN	02788	7098-4012-00
5	1250-1465	5	1	NUT-RF CONN	02788	7098-5052-15
6	04291-00634	1	1	PLATE	28480	04291-00634
7	04291-04001	4	1	BOTTOM COVER	28480	04291-04001
8	0515-0914	8	10	SCR-MACH M3×0.5	01125	-

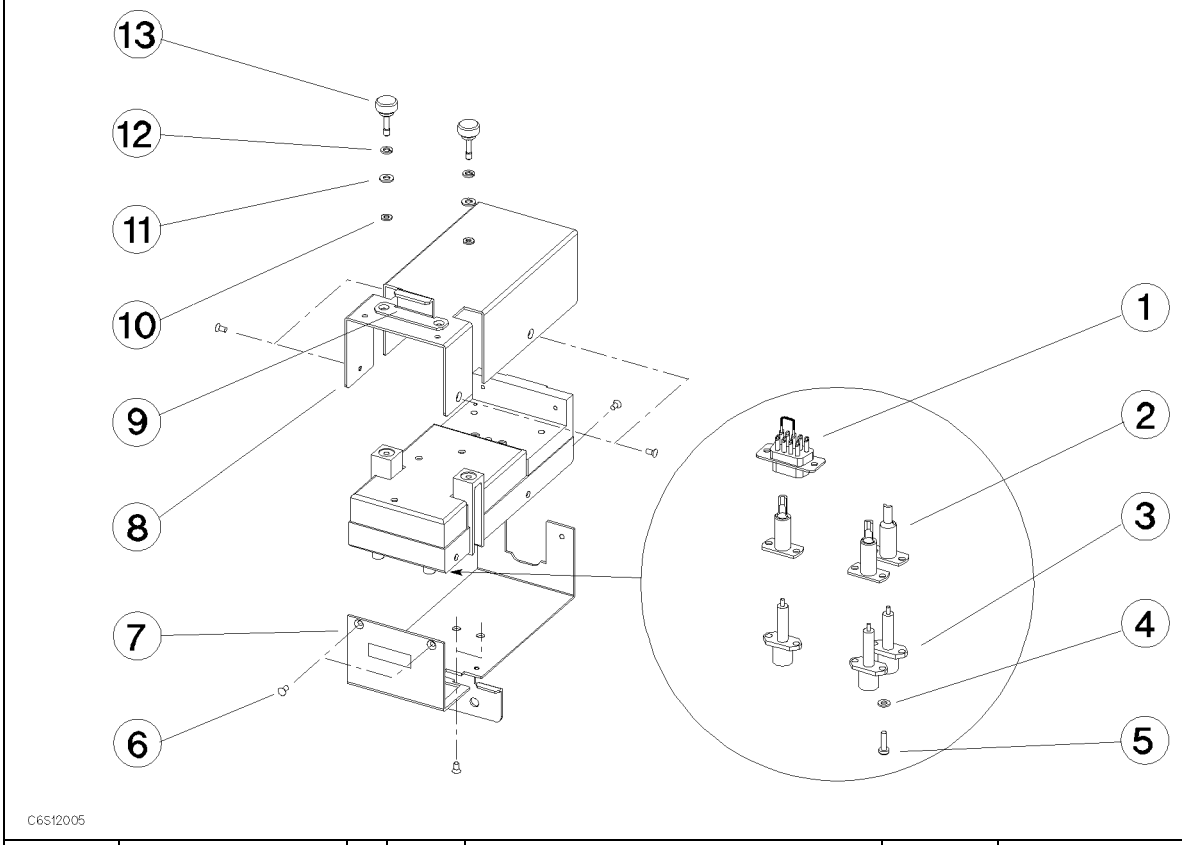
Table 12-25. High Temp. Test Heads Parts (Fixture Side, Option 014)



C6S12007

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	16190-25011	3	1	CAP, APC-7®	28480	16190-25011
2	1510-0130	1	1	B-POST	28480	1510-0130
3	04291-04006	9	1	TOP COVER	28480	04291-04006
4	1250-0820	4	1	CMPNT-RF CONN	02788	7098-4012-00
5	1250-1465	5	1	NUT-RF CONN	02788	7098-5052-15
6	04291-00636	3	1	PLATE	28480	04291-00636
7	04291-04023	0	1	BOTTOM COVER	28480	04291-04023
8	0515-0914	8	8	SCR-MACH M3×0.5	01125	-

Table 12-26.
High Temp. Test Heads Parts (Test Station Side, Opt. 013 and 014)



Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	1252-5593	2	1	ID CONNECTOR, 9PIN[1]	06369	HDE-9P(05)
2	04291-24067	4	3	SLEEVE	28480	04291-24067
3	1250-2450	0	3	RF CONNECTOR	02788	4552-1352-00
4	2190-0014	1	6	WASHER	04805	1902-00-00-2580
5	0520-0129	8	6	SCREW	01125	-
6	0515-0914	8	12	SCR-MACH M3×0.5	01125	-
7	(Not assigned)[2]		1	BOTTOM-COVER		
8	04291-04015	0	1	TOP-COVER (OPT.013)	28480	04291-04015
	04291-04025	2	1	TOP-COVER (OPT.014)	28480	04291-04025
9	04291-01282	7	1	ANGLE PLATE	28480	04291-01282
10	04291-25062	1	2	INSULATOR	28480	04291-25062
11	3050-0893	9	2	WASHER	06691	-
12	2190-0586	2	2	WASHER	06691	A2WASPSR0158
13	04291-24068	5	2	KNOB	28480	04291-24068

1 Refer to Figure 12-18 for ID connector wiring for option 013 and 014

2 Bottom cover has a serial number label, so that it cannot be replaced with a new one.

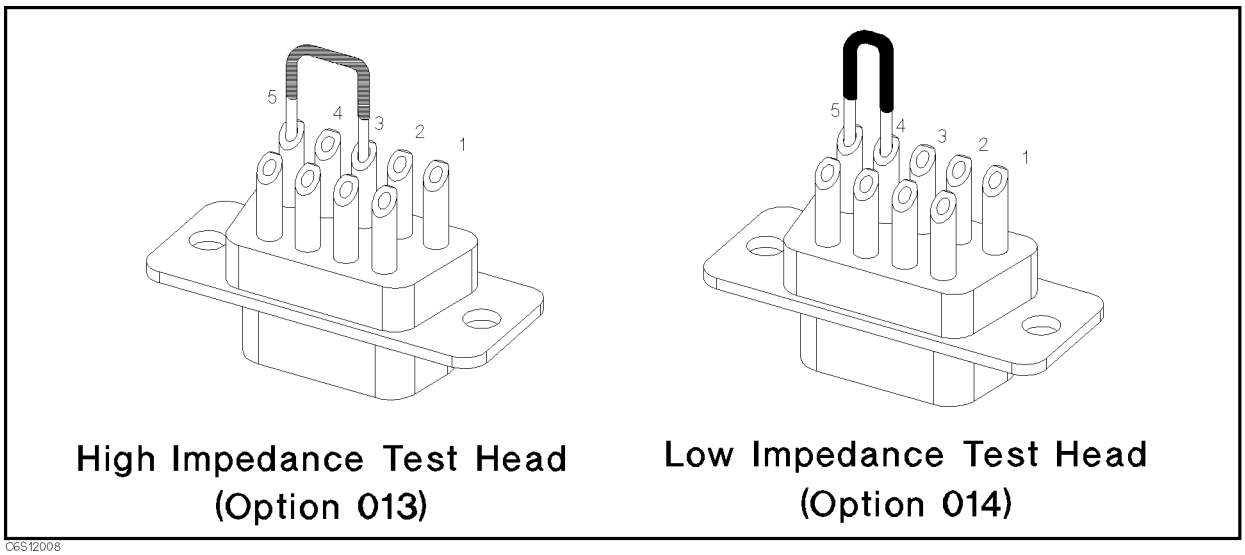
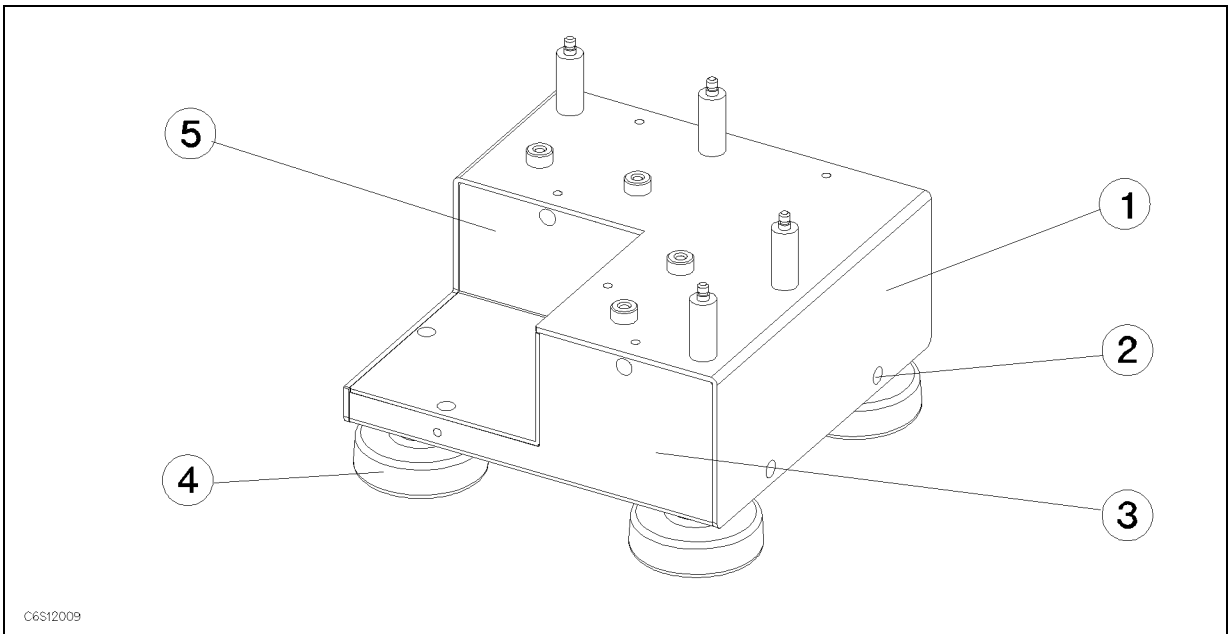


Figure 12-18. ID Connector Wiring

Table 12-27. High Temp. Test Heads Parts (Fixture Stand)



Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	04291-04081	0	1	COVER TOP	28480	04291-04081
2	0515-0914	8	11	SCR-MACH M3×0.5	01125	-
3	04291-04082	1	1	COVER BOTTOM	28480	04291-04082
4	04291-25081	4	4	FOOT	28480	04291-25081
	3050-0893	9	4	WASHER-FL MTLC (FOR FOOT)	06691	-
	0515-1718	2	4	SCR-MACHINE (FOR FOOT)	01125	-
5	04291-04083	2	1	COVER	28480	04291-04083
—	04291-60121	7	1	FIXTURE STAND[1]	28480	04291-60121

1 The entire part.

13

Replacement Procedures

INTRODUCTION

This chapter describes how to replace the analyzer's major assemblies. The cover and panel removal procedures that are required for some assembly replacements are described first. Then the replacement procedures for each major assembly is described.

TOP COVER REMOVAL

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #2 (medium)

Procedure

1. Disconnect the power cable from the analyzer.
2. Remove the two rear feet behind the top cover.
3. Loosen the top cover rear screw.
4. Slide the top cover toward the rear and lift it off.

BOTTOM COVER REMOVAL

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #2 (medium)

Procedure

1. Disconnect the power cable from the analyzer.
2. Place the analyzer upside down.
3. Remove the two rear feet behind the bottom cover.
4. Loosen the bottom cover rear screw.
5. Slide the bottom cover toward the rear and lift it off.

SIDE COVER REMOVAL

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #2 (medium)

Procedure

1. Remove the top cover as described in the "TOP COVER REMOVAL" procedure.
2. Remove the bottom cover as described in the "BOTTOM COVER REMOVAL" procedure.
3. Remove the two screws at the side strap handle caps to remove the strap.
4. Slide off the side cover toward the rear.
5. For the other side cover, repeat steps 3 and 4.

FRONT PANEL REMOVAL

Tools Required

- Pozidriv screwdriver, pt size #2 (medium)
- Flat blade screwdriver.

Procedure

1. Place the analyzer upside down.
2. Remove two front feet.
3. Remove four screws from the bottom of the front frame.
4. Turn the analyzer over into the correct position.
5. Remove the top trim strip from the front frame by prying the trim strip up with a flat screwdriver.
6. Remove six screws from the top of the front frame.
7. Gently pull the front panel knob to remove the front panel assembly from the front frame.

REAR PANEL REMOVAL

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdrivers, pt size #1 (small), size #2 (medium)

Procedure

1. Remove the top, bottom, and side covers as described in the "SIDE COVER REMOVAL" procedure.
2. Place the analyzer upside down.
3. Remove four screws from the bottom of the rear frame.
4. Turn the analyzer over into the correct position.
5. Remove the top shield plate.
6. Disconnect the two cables (power line).
7. Remove the RF flexible cables "I" and "O" from A5 Synthesizer.
8. Remove the RF cable "V" from A60 Frequency Reference (Option 1D5.)
9. Gradually push the A40 preregulator toward the rear to pull the rear panel assembly out from the rear frame, and remove the all cables connected to the rear panel.

A1 CPU REPLACEMENT

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #1 (small) and #2 (medium)
- IC Extractor

Removal Procedure

1. Remove the bottom cover as described in the "BOTTOM COVER REMOVAL" procedure.
2. Disconnect all cables and wires from A1.
3. Remove the EEPROM from A1 (see Figure 13-1). Mount the EEPROM on the replacement A1.

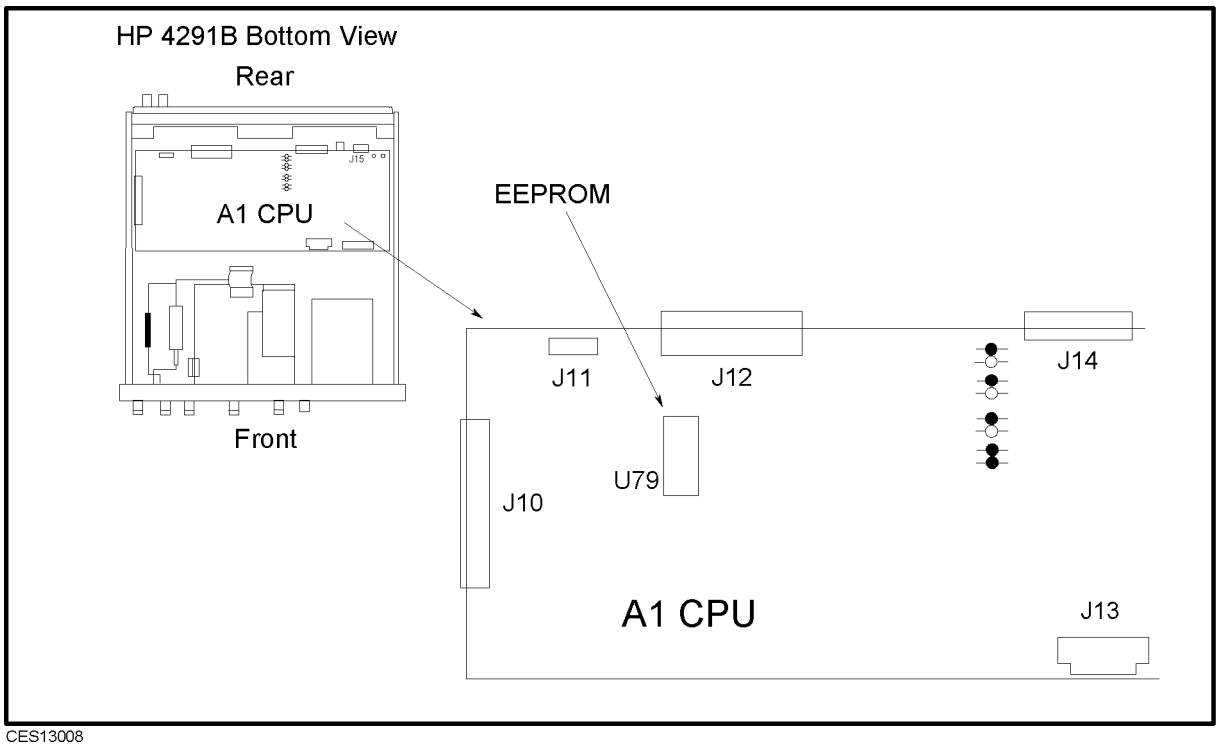


Figure 13-1. A1 EEPROM Location

Note When using a re-built A1, return the defective A1 with the EEPROM originally mounted on the re-built A1.

4. Remove all screws from A1 to remove A1 from the chassis.

Replacement Procedure

1. Place the replacement A1 on the analyzer.
2. Attach A1 with the screws removed in the “Removal Procedure” procedure.
3. Connect all cables disconnected in the “Removal Procedure” to A1.
4. Replace the bottom cover.

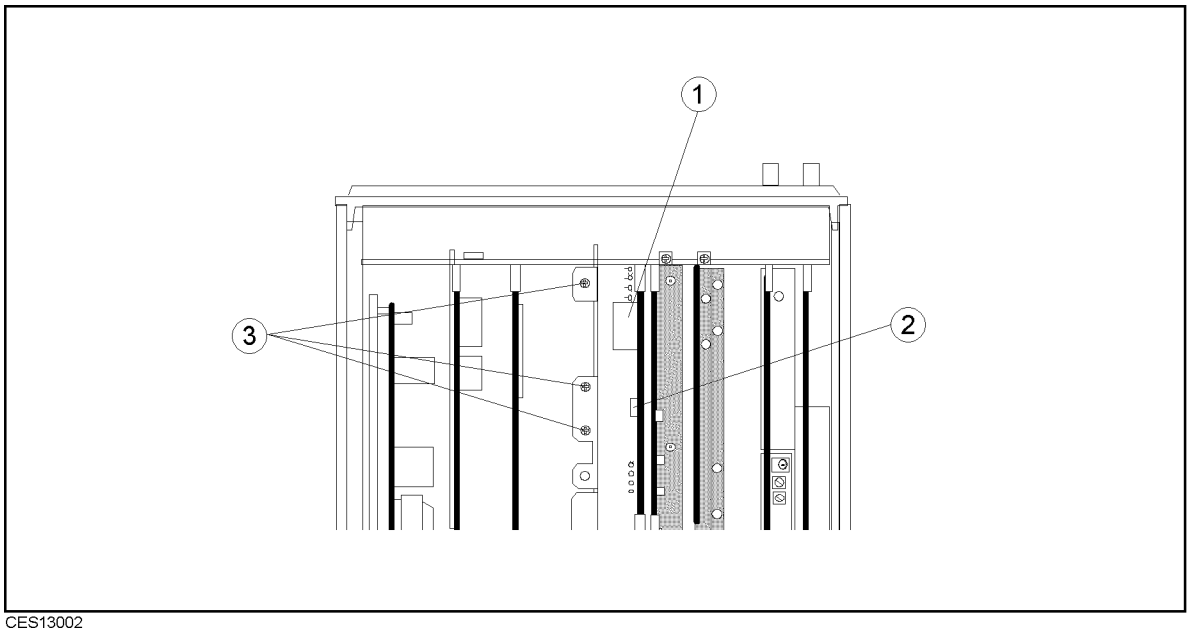
A2 POST REGULATOR REPLACEMENT

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #1 (small)

Removal Procedure

1. Remove the top cover as described in the "TOP COVER REMOVAL" procedure.
2. Remove the top shield plate.
3. Disconnect the wire designated ① in Figure 13-2.
4. Disconnect the wire designated ② in Figure 13-2, if the option 1D5 is installed.



CES13002

Figure 13-2. A2 Post Regulator Replacement

5. Remove the three screws designated ③ in Figure 13-2.
6. Lift the extractors at the top of A2, and lift A2 out.

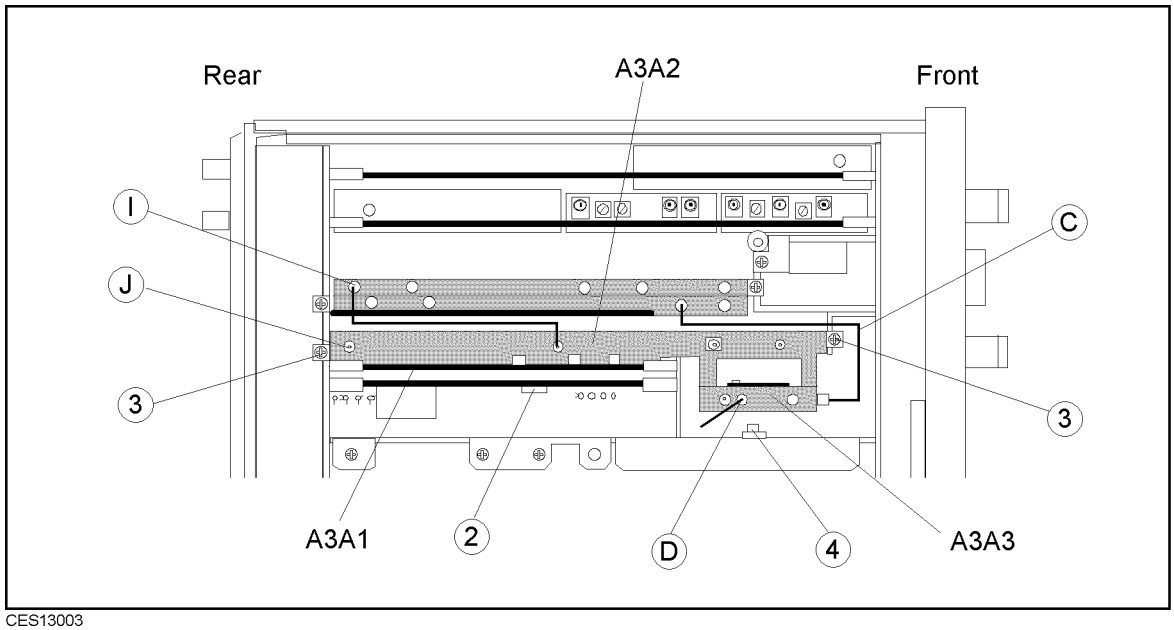
A3A1 Source Vernier, A3A2 SECOND LO, AND A3A3 SOURCE REPLACEMENT

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #1 (small) and #2 (medium)
- Open-end wrench, 1/4 inch and 5/16 inch

Removal Procedure

1. Remove the top cover as described in the "TOP COVER REMOVAL" procedure.
2. Remove the top shield plate.
3. Remove the semi rigid cables Ⓒ and ① completely from the analyzer.



CES13003

Figure 13-3. A3 Replacement

4. Remove the semi rigid cable Ⓓ from A3A3, and clamp the cable with the cable clamp designated ④ in Figure 13-3. (The cable needs to be clamped so that the cable is not caught by A3 when A3 is lifted out.)
5. Disconnect the flexible cable Ⓙ from A3A1.
6. Disconnect the wire designated ② in Figure 13-3, if the option 1D5 is installed.
7. Remove the two screws designated ③ in Figure 13-3.
8. Lift the extractors at the top of A3A1, and lift A3 out.
9. *—A3A1 Removal—*
   a. Remove all cables and wires from A3A1.
   b. Place A3 facing A3A1 upward as shown in Figure 13-4.

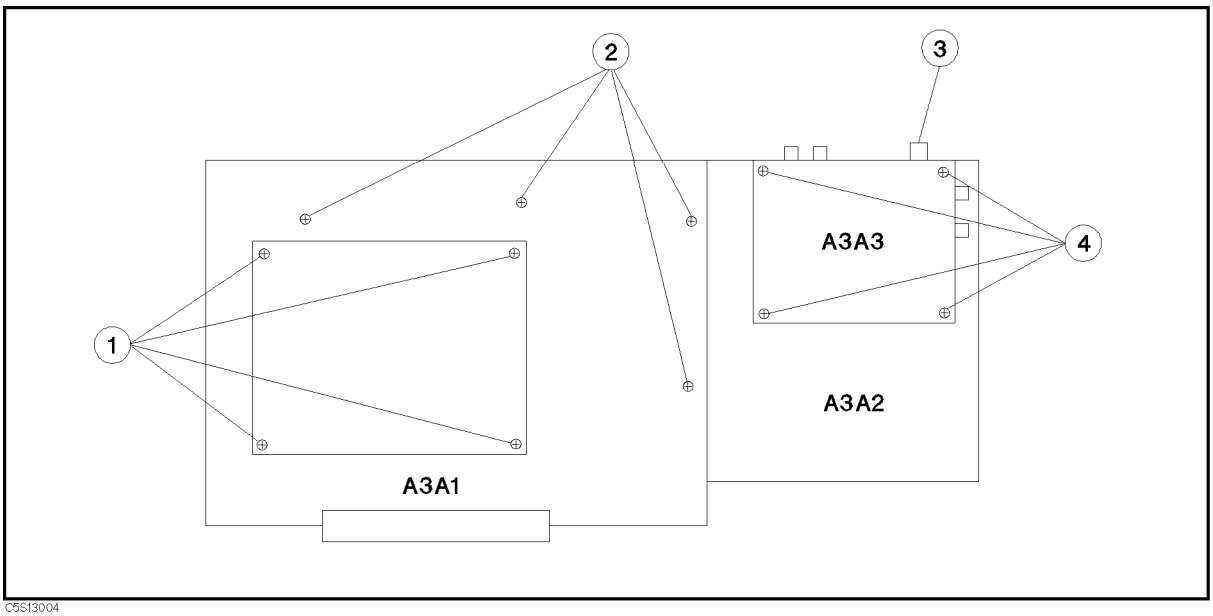


Figure 13-4. A3A1, A3A2, and A3A3 Replacement

c. Remove the four screws designated ① in Figure 13-4 to remove the shield case on A3A1.

d. Remove the four screws designated ② in Figure 13-4 to remove A3A1 from A3A2.

Note When using a re-built A3A1, return the defective A3A1 without the shield case.

10. *—A3A2 Removal—*

a. Remove all cables from A3A2.

b. Remove A3A1 as described in *A3A1 Removal.*

c. Remove A3A3 as described in *A3A3 Removal.*

d. Pull the gasket out from A3A2 shield, and install the gasket in the replacement A3A2.

Note When using a re-built A3A2, return the defective A3A2 without the gasket.

11. *—A3A3 Removal—*

a. Place A3 facing A3A2 upward as shown in Figure 13-4.

b. Remove all cables and wires from A3A3.

c. Remove the connector cover designated ③ in Figure 13-4.

d. Remove the four screws designated ④ in Figure 13-4 to remove A3A3 from A3A2.

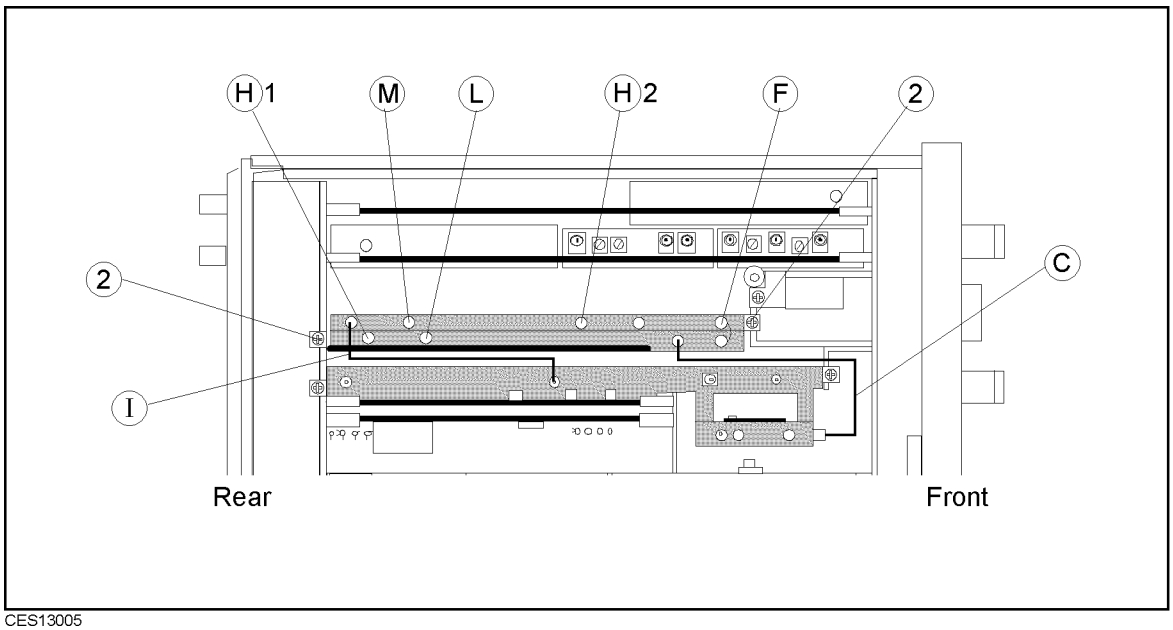
A4 FIRST LO/RECEIVER RF REPLACEMENT

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #1 (small) and #2 (medium)
- Open-end wrench, 1/4 inch and 5/16 inch

Removal Procedure

1. Remove the top cover as described in the "TOP COVER REMOVAL" procedure.
2. Remove the top shield plate.
3. Remove the semi rigid cables Ⓒ, Ⓕ and Ⓘ completely from the analyzer.



CES13005

Figure 13-5. A4 First Lo/Receiver RF Replacement

4. Disconnect the flexible cables Ⓗ$_1$, Ⓗ$_2$, Ⓛ, and Ⓜ from A4.
5. Remove the two screws designated ② in Figure 13-5, and lift A4 out.

Note A4A1 First LO and A4A2 Receiver RF must not be separated.

A5 SYNTHESIZER REPLACEMENT

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #1 (small)
- Open-end wrench, 1/4 inch

Removal Procedure

1. Remove the top cover as described in the "TOP COVER REMOVAL" procedure.
2. Remove the top shield plate.
3. Disconnect all cables from A5.
4. Lift the extractors at the top of A5, and lift A5 out.

A6 RECEIVER IF REPLACEMENT

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #1 (small)

Removal Procedure

1. Remove the top cover as described in the "TOP COVER REMOVAL" procedure.
2. Remove the top shield plate.
3. Disconnect the flexible cable Ⓜ from A6.
4. Lift the extractors at the top of A6 to disconnect the flexible cable Ⓕ from A6.
5. Lift A6 out.

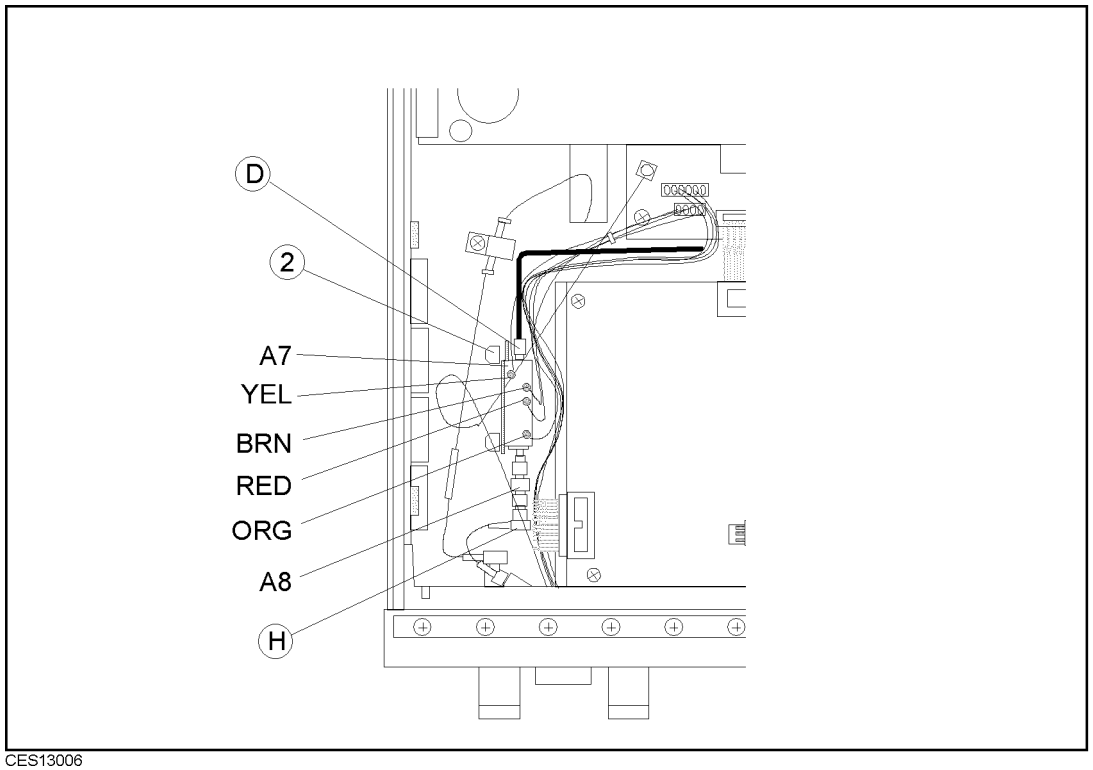
A7 OUTPUT ATT AND A8 3 dB ATT REPLACEMENT

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #1 (small) and #2 (medium)
- Open-end wrench, 5/16 inch

Removal Procedure

1. Remove the bottom cover as described in the "BOTTOM COVER REMOVAL" procedure.
2. Remove the flexible cable Ⓗ from A8.



CES13006

Figure 13-6. A7 Input ATT and A8 3 dB ATT Replacement

3. Remove A8 from A7.
4. Unsolder the cable designated ① in Figure 13-6 from the A7.
5. Remove the semi rigid cable Ⓓ from A7.
6. Remove the two screws designated ② in Figure 13-6, to remove the A7 holder from the chassis.
7. Remove the two screws to remove A7 from the holder.

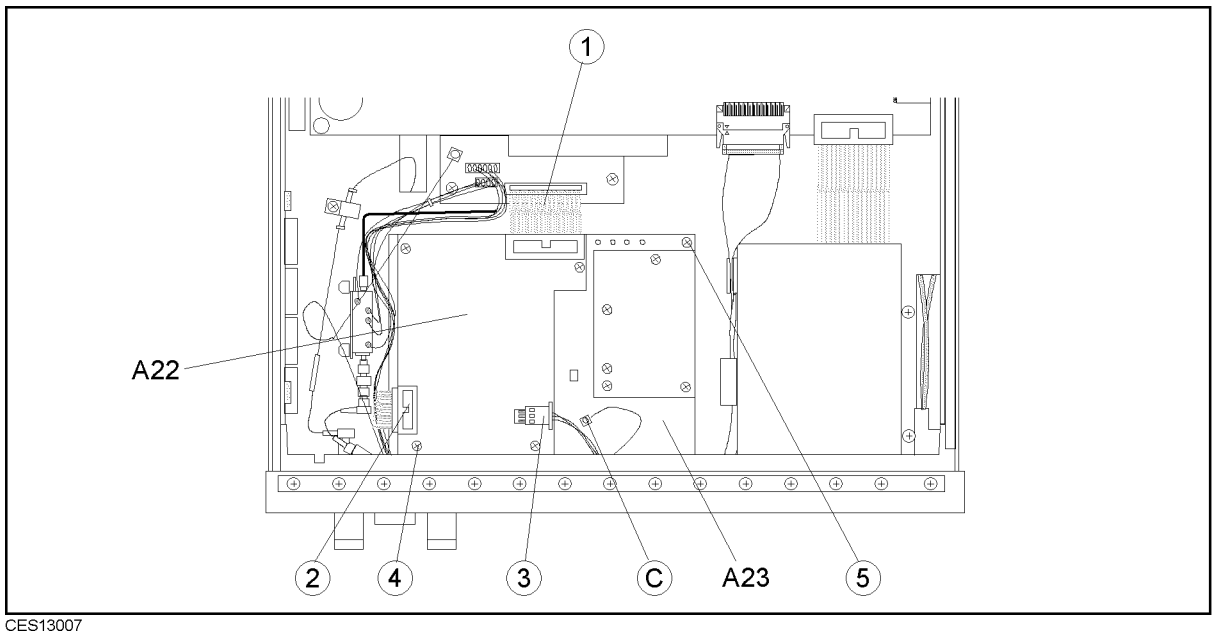
A22 DC BIAS 1/2 and A23 DC BIAS 2/2 REPLACEMENT

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #1 (small) and #2 (medium)

Removal Procedure

1. Remove the bottom cover as described in the "BOTTOM COVER REMOVAL" procedure.
2. Disconnect the flat cables and wire designated ①, ②, and ③ in Figure 13-7.



CES13007

Figure 13-7. A22/A23 DC Bias Replacement

3. Loosen the four screws designated ④ in Figure 13-7 to remove A22 from A23.
4. Disconnect the flexible cable © from A23.
5. Remove the five screws designated ⑤ in Figure 13-7 to remove A23 from the chassis.

A30 KEYBOARD REPLACEMENT

Tools Required

- Pozidriv screwdrivers, pt size #1 (small) and #2 (medium)
- Flat blade screwdriver
- Hex key, 0.063 inch across flats

Removal Procedure

1. Loosen the two hex set screws in the front panel knob, and pull the knob off.
2. Remove the front panel as described in the "FRONT PANEL REMOVAL" procedure.
3. Disconnect the flat cable assembly from A30.
4. Remove the eight screws on A30 to remove A30 from the front panel.

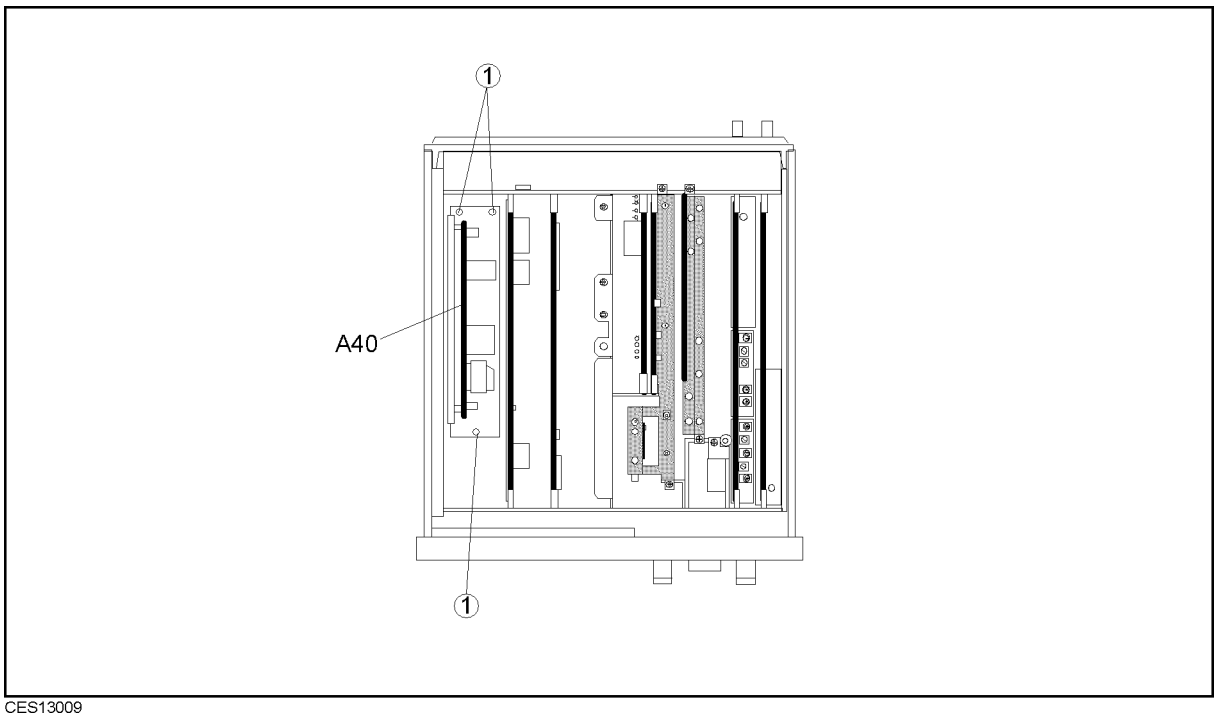
A40 PREREGULATOR REPLACEMENT

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #1 (small) and #2 (medium)

Removal Procedure

1. Remove the top cover as described in the "TOP COVER REMOVAL" procedure.
2. Remove the top shield plate.



CES13009

Figure 13-8. A40 Preregurator Replacement

3. Remove three screws designated ① in Figure 13-8
4. Lift the A40, and remove all cables from the A40.

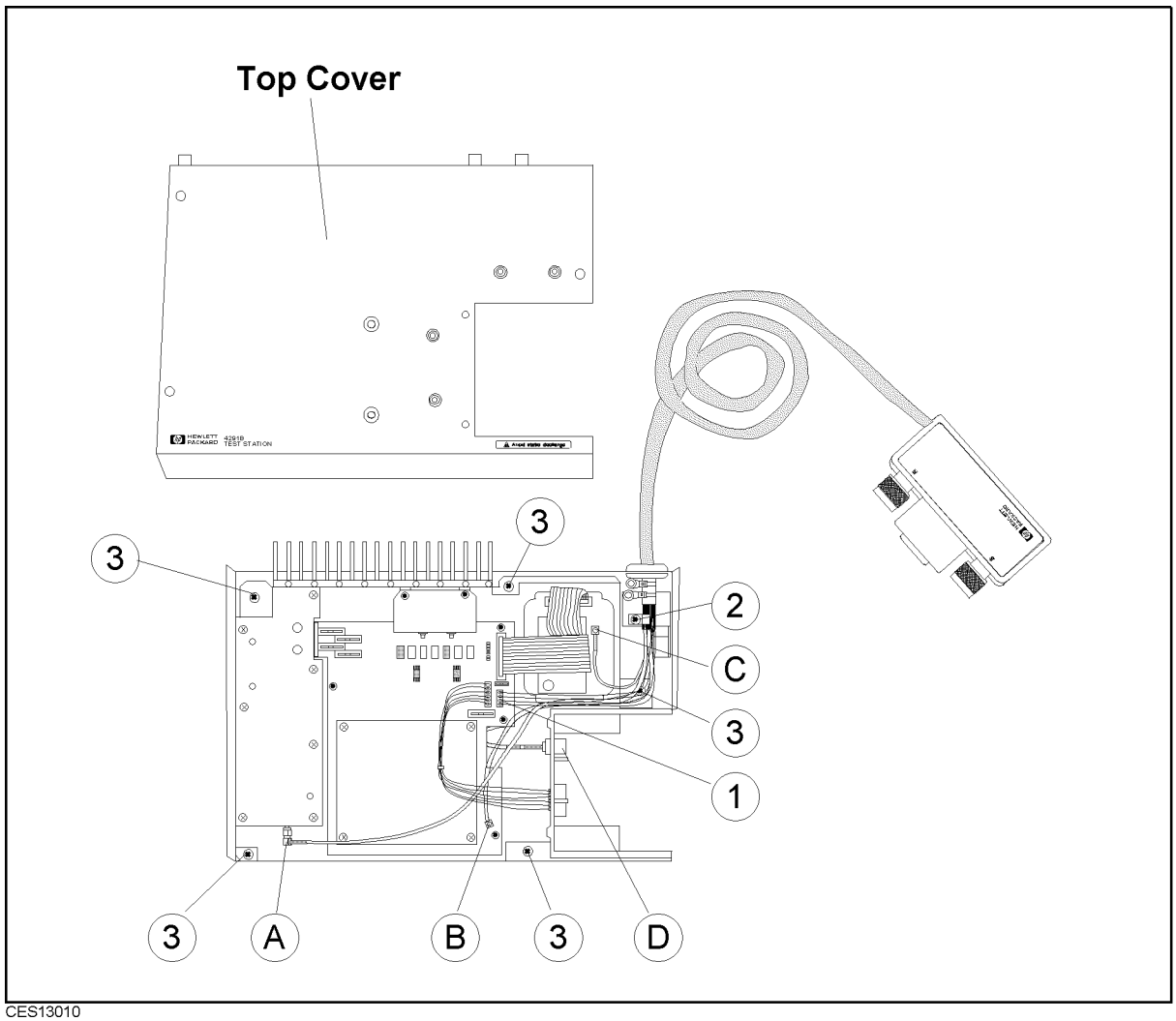
A41 TRD AMP REPLACEMENT

Tools Required

- Pozidriv screwdriver, pt size #1 (small)
- Open-end wrench 9/16 inch
- Box driver 11/32 inch

Removal Procedure

1. Remove the ten screws to remove the top cover from the test station.



CES13010

Figure 13-9. A41 TRD Amp Replacement

2. Disconnect the flexible cables Ⓐ, Ⓑ, Ⓒ ,and Ⓓ from A41.
3. Disconnect the wire designated ① in Figure 13-9.
4. Remove the screw designated ② in Figure 13-9 to remove the cable clamp.
5. Remove the five screws designated ③ in Figure 13-9 to remove A41 from the bottom cover.

A50 DC-DC CONVERTER REPLACEMENT

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #1 (small) and #2 (medium)

Removal Procedure

1. Remove the top cover as described in the "TOP COVER REMOVAL" procedure.
2. Remove the top shield plate.
3. Lift the extractors at the top of A50, and remove all cables from the A50.

A51 GSP REPLACEMENT

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #1 (small) and #2 (medium)

Removal Procedure

1. Remove the top cover as described in the "TOP COVER REMOVAL" procedure.
2. Remove the top shield plate.
3. Remove all cables from the top of A51.
4. Lift the extractors at the top of A51, and lift A51 out.

Replacement Procedure

1. Insert the new A51 into the analyzer by half.
2. Connect the flat cable from the rear to A51J
3. Connect the wire from LCD to A51.
4. Connect the flat cable from the LCD to A51, then push the A51 into the analyzer completely.

Note Marked side of flat cable has to be connected to J3 of A51, not to LCD.

5. Replace the top shield plate, and replace the top cover.

A52 LCD REPLACEMENT

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #1 (small) and #2 (medium)

Removal Procedure

1. See Front Assembly Parts in chapter 12.

A53 FDD REPLACEMENT

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #1 (small)
- Hex socket, 7/32 inch (5.5 mm)

Removal Procedure

1. Remove the bottom cover as described in the "BOTTOM COVER REMOVAL" procedure.
2. Remove the flat cable from the cable clamp on A53 holder.
3. Disconnect A53's flat cable from the A1 CPU.
4. Remove the four nuts from the A53 holder.
5. Remove A53 with holder from the chassis.
6. Remove the four screws from the holder to remove it from A53.
7. Disconnect the flat cable and wire from A53.

A60 FREQ REF REPLACEMENT

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #1 (small) and #2 (medium)

Removal Procedure

1. Remove the top cover as described in the "TOP COVER REMOVAL" procedure.
2. Remove the top shield plate.
3. Remove the screw that fix A60, and lift A60 out.
4. Remove the flexible cable from A60.
5. Remove the A60 wire from A2.

TEST HEAD REPLACEMENT

Tools Required

- Pozidriv screwdriver, pt size #1 (small)

Replacement Procedure

1. Remove the bottom covers from the defective test head and the replacement test head.
2. Replace the defective test head's bottom cover on the replacement test head.

Note

The bottom cover replacement is required to maintain the serial number label that is put on the bottom cover. The serial number label is required to identify the test head and guarantee the analyzer system specifications.

CENTER CONDUCTOR COLLET REPLACEMENT

The analyzer uses 7 mm connectors. The center conductor collets of the connectors can be replaced as usual 7 mm connectors.

- Use precision 6-slot collet (HP PN 85050-20001) as a replacement part.
- Use the removing tool guide (HP PN 04291-21002) to remove a collet from the low-loss capacitor.

Note

There are two Hewlett-Packard publications available to help you learn 7 mm connector maintenance:

- **Microwave Connector Care** (HP PN 08510-90064) explains in detail how to care for microwave connectors.
- **HP Application Note 326 Coaxial Systems** (HP PN 5954-1516) summarizes microwave connector care. It is available free from the nearest Hewlett-Packard office.

14

Post Repair Procedures

INTRODUCTION

This chapter lists the procedures required to verify the analyzer operation after an assembly is replaced with a new one.

POST REPAIR PROCEDURES

Table 14-1 *Post Repair Procedures* lists the required procedures that must be performed after the replacement of an assembly or the EEPROM. These are the recommended minimum procedures to ensure that the replacement is successfully completed.

When you replace an assembly or the EEPROM on the A1 CPU, perform the adjustments and updating correction constants (CC), then verify the analyzer performance according to Table 14-1.

For the detailed procedure of the adjustments and updating correction constants, see Chapter 3. For the detailed verification procedures, see this manual's chapter specified in Table 14-1.

Table 14-1. Post Repair Procedures

Replaced Assembly or Part	Adjustments Correction Constants (CC)	Verification
A1 CPU	Firmware Installation.[1]	*Inspect the Power On Sequence* [2] Internal Test 2: A1 VOLATILE MEMORY[3]
A1 EEPROM	Step Pretune CC OSC Level CC DC Bias Level CC	*Inspect the Power On Sequence* [2] *OSC Level Accuracy Test* [4] *DC Bias Level Accuracy Test* [4]
A2 Post-Regulator	CAL OUT Level	*Inspect the Power On Sequence* [2] Frequency Accuracy Test[4]
A3A1 Source Vernier	Source VCXO Adjustment OSC Level CC	*Inspect the Power On Sequence* [2] *OSC Level Accuracy Test* [4] External Test 25: FRONT ISOL'N[3]
A3A2 2nd LO	Second LO PLL Lock Adjustment Source Mixer Local Leakage Adjustment OSC Level CC	*Inspect the Power On Sequence* [2] *OSC Level Accuracy Test* [4] External Test 25: FRONT ISOL'N[3]

1 See the *Firmware Installation* procedure in this chapter.

2 See Chapter 4.

3 See Chapter 10.

4 See Chapter 2.

Table 14-1. Post Repair Procedures (continued)

Replaced Assembly or Part	Adjustments Correction Constants (CC)	Verification
A3A3 Source	OSC Level CC	*Inspect the Power On Sequence* [1] *OSC Level Accuracy Test* [2] External Test 25: FRONT ISOL'N[3]
A4 1st LO/Receiver RF	None	*Inspect the Power On Sequence* [1] External Test 25: FRONT ISOL'N[3]
A5 Synthesizer	40 MHz Reference Oscillator Adjustment 520 MHz Level Adjustment Comb Generator Adjustment Step Pretune CC	*Inspect the Power On Sequence* [1] Internal Test 8: A5 STEP OSC[3] *Frequency Accuracy Test* [2]
A6 Receiver IF	Source VCXO Adjustment Hold Step Adjustment Band Pass Filter Adjustment	*Inspect the Power On Sequence* [1]
A7 Output ATT	OSC Level CC	*Inspect the Power On Sequence* [1] External Test 21: OUTPUT ATTENUATOR[3] *OSC Level Accuracy Test* [2]
A8 Output 3 dB ATT	OSC Level CC	*OSC Level Accuracy Test* [2]
A9 Input 3 dB ATT	None	External Test 22: RECEIVER GAIN[3]
A20 Motherboard	None	*Inspect the Power On Sequence* [1]
A22 DC Bias 1/2	DC Bias Level CC	*Inspect the Power On Sequence* [1] *DC Bias level accuracy test* [2]
A23 DC Bias 2/2	DC Bias Level CC	*Inspect the Power On Sequence* [1] *DC Bias level accuracy test* [2]
A30 Keyboard	None	*Inspect the Power On Sequence* [1] External Test 17: FRONT PANEL DIAG.[3]
A31 I/O Connector	None None	*Inspect the Power On Sequence* [1] *Check the HP-IB Interface* [1]
A32 I-BASIC Interface	None None	*Inspect the Power On Sequence* [1] *Check the A32 I-BASIC Interface and the mini DIN Keyboard* [4]
A40 Pre-Regulator	None	Internal Test 4: A2 POST REGULATOR[3]
A41 TRD Amp	None	*Inspect the Power On Sequence* [1] External Test 12: CABLE ISOL'N[3]
Test Station Cable	None	*Inspect the Power On Sequence* [1] External Test 12: CABLE ISOL'N[3]
A50 DC-DC Converter	None	Internal Test 4: A2 POST REGULATOR[3]
A51 GSP	None	*Inspect the Power On Sequence* [1]
A52 LCD	None	*Inspect the Power On Sequence* [1]
A53 FDD	None	*Inspect the Power On Sequence* [1] External Test 18: DSK DR FAULTY ISOLN[3]
A60 High Stability Frequency Reference	10 MHz Reference Oscillator Frequency	*Inspect the Power On Sequence* [1] *Frequency Accuracy Test (Opt.1D5)* [2]

1 See Chapter 4.

2 See Chapter 2.

3 See Chapter 10.

4 See Chapter 6.

FIRMWARE INSTALLATION

No firmware is installed in new A1 CPU assembly. When you replace a faulty A1 CPU with a new one, perform the following steps to install the firmware into the A1 CPU.

Ordering the Firmware Diskette

A firmware diskette (3.5 inch) that contains the analyzer's firmware is required for the firmware installation. If you do not have a firmware diskette, you must order one. For ordering information, contact your nearest Hewlett-Packard service center and provide the revision of the analyzer's firmware. The part number of the firmware diskette depends on the firmware revision. The firmware revision of the analyzer is indicated on the revision label attached on the rear panel as shown in Figure 14-1.

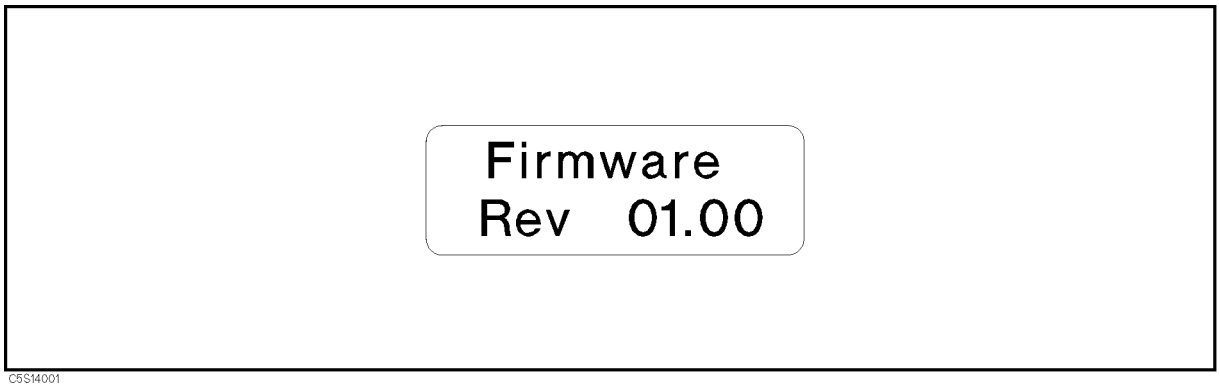
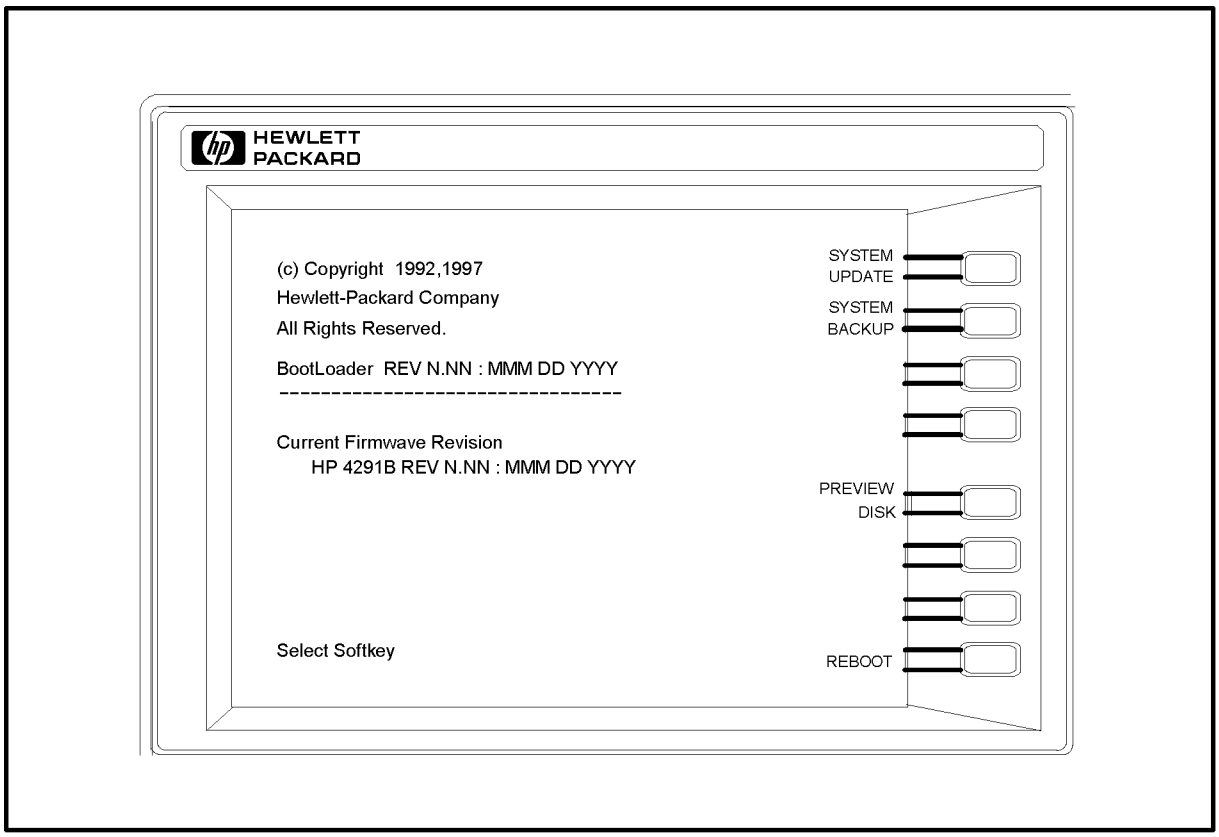


Figure 14-1. Firmware Revision Label

Installing the Firmware

Perform the following procedure to install the firmware into the analyzer.

1. Turn the analyzer power off.
2. Press the Preset key. While pressing the key, turn the analyzer power on.
3. Wait until the bootloader menu appears on the CRT as shown in Figure 14-2.



CES14002

Figure 14-2. Bootloader Menu Display

4. Insert the firmware diskette into the floppy disk drive on the front panel.
5. Press `SYSTEM UPDATE` and `CONTINUE`. The analyzer displays “Loading From Disk” and starts the firmware installation.
6. Wait until the analyzer displays “Update Complete.”
7. Press `REBOOT` or turn the analyzer power off and on. The analyzer starts the operation using the installed firmware.
8. Verify that no error message is displayed and that the revision displayed is that of the revision label.
   - In case of unexpected results, inspect the firmware diskette for any damage. Clean the built-in FDD and retry the procedure.

A

Manual Changes

Introduction

This appendix contains the information required to adapt this manual to earlier versions or configurations of the HP 4291B than the current printing date of this manual. The information in this manual applies directly to the HP 4291B RF Impedance/Material Analyzer serial number prefix listed on the title page of this manual.

Manual Changes

To adapt this manual to your HP 4291B, refer to Table A-1 and Table A-2, and make all of the manual changes listed opposite your instrument's serial number and firmware version.

Instruments manufactured after the printing of this manual may be different than those documented in this manual. Later instrument versions will be documented in a manual changes supplement that will accompany the manual shipped with that instrument. If your instrument's serial number is not listed on the title page of this manual or in Table A-1, it may be documented in a *yellow MANUAL CHANGES* supplement.

Turn on the line switch or execute the "`*IDN?`" command by HP-IB to confirm the firmware version. See *Programming Manual* for information on the "`*IDN?`" command. For additional information on serial number coverage, see front page of the *Operation Manual.*

Table A-1. Manual Changes by Serial Number

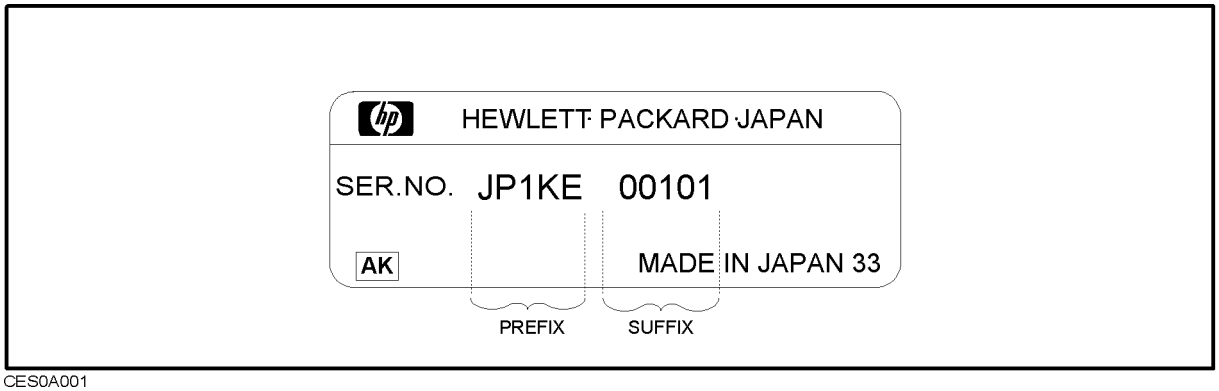
Serial Prefix or Number	Make Manual Changes
JP1KE	None

Table A-2. Manual Changes by Firmware Version

Version	Make Manual Changes
1.00 and below	None

Serial Number

Hewlett-Packard uses a two-part, ten-character serial number that is stamped on the serial number plate (see Figure A-1) attached to the rear panel. The first five digits are the serial prefix and the last five digits are the suffix.



CES0A001

Figure A-1. Serial Number Plate

Power Requirement

⚠Replacing Fuse

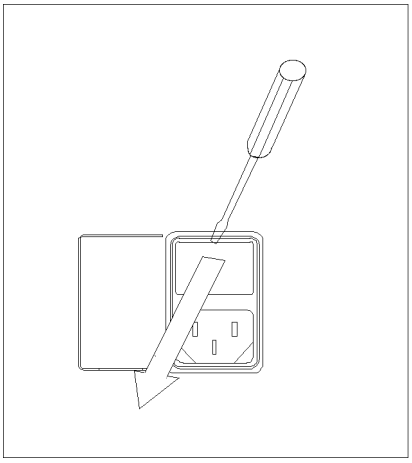
Fuse Selection

Select proper fuse according to the Table B-1.

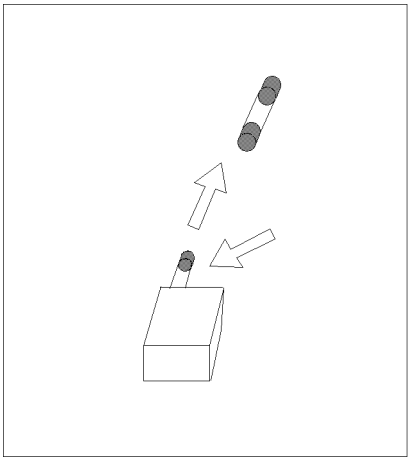
Table B-1. Fuse Selection

Fuse Rating/Type	Fuse Part Number
5A 250Vac UL/CSA type Time Delay	2110-0030

For ordering the fuse,contact your nearest Hewlett-Packard Sales and Service Office.



Open the cover of AC line receptacle on the rear panel using a small minus screwdriver.



To check or replace the fuse, pull the fuse holder and remove the fuse. To reinstall the fuse, insert a fuse with the proper rating into the fuse holder.

Power Requirements

The HP 4291B requires the following power source:

Voltage : 90 to 132 Vac, 198 to 264 Vac

Frequency : 47 to 63 Hz

Power : 300 VA maximum

Power Cable

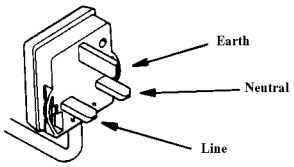
In accordance with international safety standards, this instrument is equipped with a three-wire power cable. When connected to an appropriate ac power outlet, this cable grounds the instrument frame.
The type of power cable shipped with each instrument depends on the country of destination. Refer to Figure B-1 for the part numbers of the power cables available.

Warning

For protection from electrical shock, the power cable ground must not be defeated.

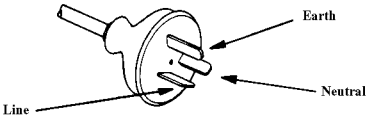
The power plug must be plugged into an outlet that provides a protective earth ground connection.

OPTION 900 United Kingdom



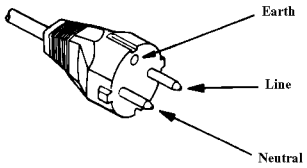
Plug : BS 1363A, 250V
Cable : HP 8120-1351

OPTION 901 Australia / New Zealand



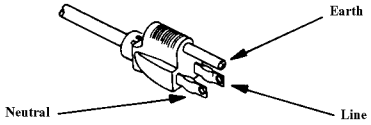
Plug : NZSS 198/AS C112, 250V
Cable : HP 8120-1369

OPTION 902 European Continent



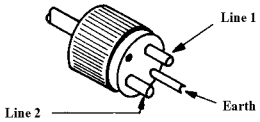
Plug : CEE-VII, 250V
Cable : HP 8120-1689

OPTION 903 U.S. / Canada



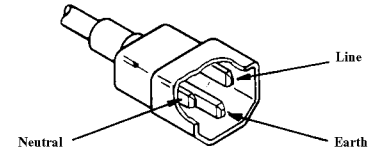
Plug : NEMA 5-15P, 125V, 15A
Cable : HP 8120-1378

OPTION 904 U.S. / Canada



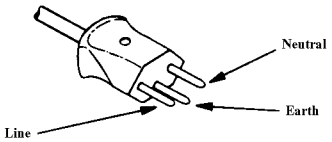
Plug : NEMA 6-15P, 250V, 15A
Cable : HP 8120-0698

OPTION 905* Any country



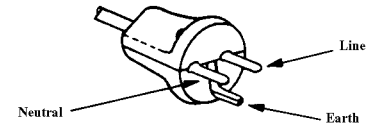
Plug : CEE 22-VI, 250V
Cable : HP 8123-1396

OPTION 906 Switzerland



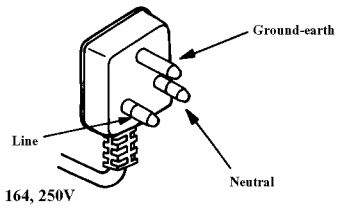
Plug : SEV 1011.1959-24507 Type 12, 250V
Cable : HP 8120-2104

OPTION 912 Denmark



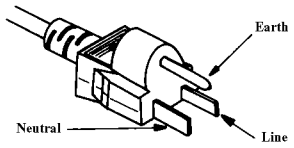
Plug : DHCR 107, 220V
Cable : HP 8120-2956

OPTION 917 India / Republic of S.Africa



Plug : SABS 164, 250V
Cable : HP 8120-4211

OPTION 918 Japan



Plug : JIS C 8303, 125V, 15A
Cable : HP 8120-4753

NOTE: Each option number includes a 'family' of cords and connectors of varoius materials and plug body configurations (straight, 90° etc.).

* Plug option 905 is frequently used for interconnecting system components and peripherals.

Figure B-1. Power Cable Supplied

Error Messages

This section lists the service related error messages that may be displayed on the analyzer display or transmitted by the instrument over HP-IB. Each error message is accompanied by an explanation, and suggestions are provided to help in solving the problem.

When displayed, error messages are usually preceded with the word CAUTION:. That part of the error message has been omitted here for the sake or brevity. Some messages are for information only, and do not indicate an error condition. Two listings are provided: the first is in alphabetical order, and the second in numerical order.

Error Messages in Alphabetical Order

222 **1st LO OSC TEST FAILED**

The 1st LO OSC (first local oscillator) on the A4A1 1st LO does not work properly. This message is displayed when an internal test 9: A4A1 1ST LO OSC fails. Troubleshoot the source group in accordance with Chapter 7.

223 **2nd LO OSC TEST FAILED**

The 2nd LO OSC (second local oscillator) on the A3A2 2nd LO does not work properly. This message is displayed when an internal test 10: A3A2 2ND LO fails. Troubleshoot the source group in accordance with Chapter 7.

225 **3rd LO OSC TEST FAILED**

The 3rd LO OSC (third local oscillator) on the A6 receiver IF does not work properly. This message is displayed when an internal test 12: A6 3RD LO OSC fails. Troubleshoot the receiver group in accordance with Chapter 8.

224 **A3 DIVIDER OUTPUT FREQUENCY OUT OF SPEC**

The output frequency of the divider circuit on the A3A1 ALC is out of its limits. This message is displayed when an internal test 11: A3A1 DIVIDER fails. Troubleshoot the source group in accordance with Chapter 7.

243 **A6 GAIN TEST FAILED**

An “external test 23: A6 GAIN” fails. Replace the A6 receiver IF. See Chapter 8.

244 **A6 VI NORMALIZER TEST FAILED**

An “external test 24: A6 VI NORMALIZER” fails. Replace the A6 receiver IF. See Chapter 8.

200 **ALL INT TEST FAILED**

This message is displayed when an internal test 0: ALL INT fails. Troubleshoot the analyzer in accordance with Chapter 4.

202 **BACKUP SRAM CHECK SUM ERROR**

The data (HP-IB Address and so on) stored in the A1 CPU's BACKUP SRAM are invalid. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

240 **CABLE ISOL'N TEST FAILED**

An "external test 27: " fails. Troubleshoot the transducer group in accordance with Chapter 9 .

190 **CORR. CONST. DATA LOST; DEFAULT DATA IS USED**

This message is displayed when the correction constants EEPROM data is lost and turned on in the service mode. Troubleshoot the analyzer in accordance with Chapter 6 .

212 **CPU BACKUP SRAM R/W ERROR**

The A1 CPU's BACKUP SRAM does not work properly. This message is displayed when an internal test 2: A1 VOLATILE MEMORY fails. Replace the A1 CPU with a new one. See Chapter 6 .

211 **CPU INTERNAL SRAM R/W ERROR**

The A1 CPU's internal SRAM does not work properly. This message is displayed when an internal test 2: A1 VOLATILE MEMORY fails. Replace the A1 CPU with a new one. See Chapter 6 .

229 **DC BIAS TEST FAILED**

The DC bias level is out of limits. This message is displayed when an "internal test 16: DC BIAS" fails. Troubleshoot the source group in accordance with Chapter 7.

204 **DSP CHIP TEST FAILED**

The A1 CPU's DSP (Digital Signal Processor) does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

213 **DSP SRAM R/W ERROR**

The DSP's SRAM on the A1 CPU does not work properly. This message is displayed when an internal test 2: A1 VOLATILE MEMORY fails. Replace the A1 COU with a new one. See Chapter 6 .

214 **DUAL PORT SRAM R/W ERROR**

The DSP's dual port SRAM on the A1 CPU does not work properly. This message is displayed when an internal test 2: A1 VOLATILE MEMORY fails. Replace the A1 CPU with a new one. See Chapter 6 .

203 **EEPROM CHECK SUM ERROR**

The data (Correction Constants and so on) stored in the A1 CPU's EEPROM are invalid. This message is displayed when an internal test 1: A1 CPU fails. Troubleshoot the A1 CPU in accordance with Chapter 6 .

199 **EEPROM WRITE ERROR**

Data cannot be stored properly into the EEPROM on the A1 CPU. This message is displayed when performing the display background adjustment or updating correction constants in the EEPROM using the adjustment program. Troubleshoot the A1 CPU in accordance with Chapter 6 .

205 **F-BUS TIMER CHIP TEST FAILED**

The A1 CPU's F-BUS (Frequency Bus) timer does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

218 **FAILURE FOUND FROM A/D MUX TO A/D CONVERTER**

A trouble is found on the signal path from the A/D multiplexer to A/D converter on the A6 receiver IF. This message is displayed when an internal test 5: A6 A/D CONVERTER fails. Troubleshoot the A6 receiver IF in accordance with Chapter 8.

217 **FAN POWER OUT OF SPEC**

The voltage of the fan power supply at the DC bus node 11 is out of its limits. This message is displayed when an internal test 4: A2 POST REGULATOR fails. Troubleshoot the power supply functional group in accordance with Chapter 5.

208 **FDC CHIP TEST FAILED**

The A1 CPU's FDC (Flexible Disk drive control) ship does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

201 **FLASH MEMORY CHECK SUM ERROR**

The data (Firmware) stored in the A1 flash memory are invalid. This message is displayed in the bootloader menu. Troubleshoot the A1 CPU in accordance with Chapter 6 .

230 **FLOPPY DISK DRIVE FAILURE FOUND**

The A53 built-in FDD (floppy disk drive) does not work properly. This message is displayed when an external test 18: DSK DR FAULT ISOL'N fails. Replace the A53 FDD with a new one. See Chapter 6 .

220 **FRACTIONAL N OSC TEST FAILED**

The fractional N oscillator on the A5 synthesizer does not work properly. This message is displayed when an internal test 7: A5 FRACTIONAL N OSC fails. Troubleshoot the source group in accordance with Chapter 7.

239 **FRONT ISOL'N TEST FAILED**

An "external test 25: FRONT ISOL'N" fails. Troubleshoot the receiver group in accordance with Chapter 8.

216 **GND LEVEL OUT OF SPEC**

The voltage of the GND (Ground) at the DC bus node 26 is out of its limits. This message is displayed when an internal test 4: A2 POST REGULATOR fails. Troubleshoot the power supply functional group in accordance with Chapter 5.

237 **HI Z HEAD TEST FAILED**

An "external test 30: HIGH Z HEAD" fails. Replace the high impedance test head. See Chapter 9 .

210 **HP-HIL CHIP TEST FAILED**

The A1 CPU's HP-HIL control chip does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

209 **HP-IB CHIP TEST FAILED**

The A1 CPU's HP-IB chip does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

207 **KEY CHIP TEST FAILED**

The A1 CPU's front keyboard control chip does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

238 **LO Z HEAD TEST FAILED**

An "external test 31: LOW Z HEAD" fails. Replace the low impedance test head. See Chapter 9 .

245 **MAX VCXO LEVEL OUT OF SPEC**

Maximum VCXO level is incorrect, in performing an "adjustment test 36: 3RD VCXO LEVEL ADJ" or an "adjustment test 39: SOURCE VCXO LEVEL ADJ". In the 3RD VCXO LEVEL ADJ, replace the A6 receiver IF. In the SOURCE VCXO LEVEL ADJ, replace the A3A1 source vernier.

233 **OUTPUT ATTENUATOR TEST FAILED**

An "external test 21: OUTPUT ATTENUATOR" fails. Troubleshoot the A7 output attenuator in accordance with Chapter 7.

40 **PHASE LOCK LOOP UNLOCKED**

A phase lock loop (PLL) circuits within the analyzer does not work properly. Troubleshoot the analyzer in accordance with Chapter 6 . When a **Svc** annotation is displayed (Service Modes are activated), this error message does not appear even if a PLL circuit is not working.

215 **POST REGULATOR OUTPUT VOLTAGE OUT OF SPEC A power supply voltage of the A2 post-regulator is out of its limits. This message is displayed when an internal test 4: A2 POST REGULATOR fails. Troubleshoot the power supply functional group in accordance with Chapter 5.**

POWER FAILED ON—-

Power failure occurs on the power lines listed in the message. One or some of +65 V, +15 V, +5 V, –5 V, –15 V, and PostRegHot, follow the message. Troubleshoot the power supply functional group in accordance with Chapter 5.

198 **POWER ON TEST FAILED**

An internal test fails in the power on sequence. This message is displayed when the power on selftest fails. Troubleshoot the analyzer in accordance with Chapter 4.

231 **POWER SWEEP LINEARITY OUT OF SPEC**

This message is displayed when an external test 19: POWER SWEEP LINEARITY fails. Troubleshoot the analyzer in accordance with Chapter 4.

242 **RECEIVER GAIN OUT OF SPEC**

An "external test 25: FRONT ISOL'N" fails. A6 receiver IF gain is incorrect. Troubleshoot the receiver group in accordance with Chapter 8.

241 **RECEIVER GAIN TEST FAILED**

An "external test 22: RECEIVER GAIN" fails. Troubleshoot the receiver group in accordance with Chapter 8.

219 **REF OSC TEST FAILED**

The reference oscillator on the A5 synthesizer does not work properly. This message is displayed when an internal test 6: A5 REFERENCE OSC fails. Troubleshoot the source group in accordance with Chapter 7.

206 **RTC CHIP TEST FAILED**

The A1 CPU's RTC (Real Time Clock) does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

227 **SAMPLE FREQUENCY OUT OF SPEC**

The sampling frequency of the sample/hold circuit on the A6 receiver IF is out of its limits. This message is displayed when an internal test 15: A6 SEQUENCER fails. Troubleshoot the receiver group in accordance with Chapter 8.

228 **SOURCE LEVEL TEST FAILED**

The source level output from the A3A3 source is out of limits. This message is displayed when an "internal test 15: SOURCE LEVEL" fails. Troubleshoot the source group in accordance with Chapter 7.

232 **SOURCE FLATNESS TEST FAILED**

An "external test 20: SOURCE FLATNESS" fails. Troubleshoot the source group in accordance with Chapter 7.

226 **SOURCE OSC TEST FAILED**

The source oscillator on the A3A1 ALC does not work properly. This message is displayed when an internal test 13: A3A1 SOURCE OSC fails. Troubleshoot the source group in accordance with Chapter 7.

221 **STEP OSC TEST FAILED**

The step oscillator on the A5 synthesizer does not work properly. This message is displayed when an internal test 8: A5 STEP OSC fails. Troubleshoot the source group in accordance with Chapter 7.

235 **TRD ISOL'N I TO V TEST FAILED**

An "external test 28: TRD ISOL'N I TO V" fails. Troubleshoot the transducer group in accordance with Chapter 7.

236 **TRD ISOL'N V TO I TEST FAILED**

An "external test 29: TRD ISOL'N V TO I" fails. Troubleshoot the transducer group in accordance with Chapter 9 .

234 **TRD LOSS TEST FAILED**

An "external test 22: TRD LOSS" fails. Troubleshoot transducer group in accordance with Chapter 9 .

246 **VCXO TUNING VOLTAGE OUT OF LIMIT**

VCXO tuning voltage is incorrect, in performing an "adjustment test 36: 3RD VCXO LEVEL ADJ" or an "adjustment test 39: SOURCE VCXO LEVEL ADJ". In the 3RD VCXO LEVEL ADJ, replace the A6 receiver IF. In the SOURCE VCXO LEVEL ADJ, replace the A3A1 source vernier.

Error Messages in Numerical Order

POWER FAILED ON—-

Power failure occurs on the power lines listed in the message. One or some of +65 V, +15 V, +5 V, −5 V, −15 V, and PostRegHot, follow the message. Troubleshoot the power supply functional group in accordance with Chapter 5.

40 **PHASE LOCK LOOP UNLOCKED**

A phase lock loop (PLL) circuits within the analyzer does not work properly. Troubleshoot the analyzer in accordance with Chapter 6 . When a **Svc** annotation is displayed (Service Modes are activated), this error message does not appear even if a PLL circuit is not working.

190 **CORR. CONST. DATA LOST; DEFAULT DATA IS USED**

This message is displayed when the correction constants EEPROM data is lost and turned on in the service mode. Troubleshoot the analyzer in accordance with Chapter 6 .

198 **POWER ON TEST FAILED**

An internal test fails in the power on sequence. This message is displayed when the power on selftest fails. Troubleshoot the analyzer in accordance with Chapter 4.

199 **EEPROM WRITE ERROR**

Data cannot be stored properly into the EEPROM on the A1 CPU. This message is displayed when performing the display background adjustment or updating correction constants in the EEPROM using the adjustment program. Troubleshoot the A1 CPU in accordance with Chapter 6 .

200 **ALL INT TEST FAILED**

This message is displayed when an internal test 0: ALL INT fails. Troubleshoot the analyzer in accordance with Chapter 4.

201 **FLASH MEMORY CHECK SUM ERROR**

The data (Firmware) stored in the A1 flash memory are invalid. This message is displayed in the bootloader menu. Troubleshoot the A1 CPU in accordance with Chapter 6 .

202 **BACKUP SRAM CHECK SUM ERROR**

The data (HP-IB Address and so on) stored in the A1 CPU's BACKUP SRAM are invalid. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

203 **EEPROM CHECK SUM ERROR**

The data (Correction Constants and so on) stored in the A1 CPU's EEPROM are invalid. This message is displayed when an internal test 1: A1 CPU fails. Troubleshoot the A1 CPU in accordance with Chapter 6 .

204 **DSP CHIP TEST FAILED**

The A1 CPU's DSP (Digital Signal Processor) does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

205 **F-BUS TIMER CHIP TEST FAILED**

The A1 CPU's F-BUS (Frequency Bus) timer does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

206 **RTC CHIP TEST FAILED**

The A1 CPU's RTC (Real Time Clock) does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

207 **KEY CHIP TEST FAILED**

The A1 CPU's front keyboard control chip does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

208 **FDC CHIP TEST FAILED**

The A1 CPU's FDC (Flexible Disk drive control) ship does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

209 **HP-IB CHIP TEST FAILED**

The A1 CPU's HP-IB chip does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

210 **HP-HIL CHIP TEST FAILED**

The A1 CPU's HP-HIL control chip does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

211 **CPU INTERNAL SRAM R/W ERROR**

The A1 CPU's internal SRAM does not work properly. This message is displayed when an internal test 2: A1 VOLATILE MEMORY fails. Replace the A1 CPU with a new one. See Chapter 6 .

212 **CPU BACKUP SRAM R/W ERROR**

The A1 CPU's BACKUP SRAM does not work properly. This message is displayed when an internal test 2: A1 VOLATILE MEMORY fails. Replace the A1 CPU with a new one. See Chapter 6 .

213 **DSP SRAM R/W ERROR**

The DSP's SRAM on the A1 CPU does not work properly. This message is displayed when an internal test 2: A1 VOLATILE MEMORY fails. Replace the A1 COU with a new one. See Chapter 6 .

214 DUAL PORT SRAM R/W ERROR

The DSP's dual port SRAM on the A1 CPU does not work properly. This message is displayed when an internal test 2: A1 VOLATILE MEMORY fails. Replace the A1 CPU with a new one. See Chapter 6 .

215 POST REGULATOR OUTPUT VOLTAGE OUT OF SPEC

A power supply voltage of the A2 post-regulator is out of its limits. This message is displayed when an internal test 4: A2 POST REGULATOR fails. Troubleshoot the power supply functional group in accordance with Chapter 5.

216 GND LEVEL OUT OF SPEC

The voltage of the GND (Ground) at the DC bus node 26 is out of its limits. This message is displayed when an internal test 4: A2 POST REGULATOR fails. Troubleshoot the power supply functional group in accordance with Chapter 5.

217 FAN POWER OUT OF SPEC

The voltage of the fan power supply at the DC bus node 11 is out of its limits. This message is displayed when an internal test 4: A2 POST REGULATOR fails. Troubleshoot the power supply functional group in accordance with Chapter 5.

218 FAILURE FOUND FROM A/D MUX TO A/D CONVERTER

A trouble is found on the signal path from the A/D multiplexer to A/D converter on the A6 receiver IF. This message is displayed when an internal test 5: A6 A/D CONVERTER fails. Troubleshoot the A6 receiver IF in accordance with Chapter 8.

219 REF OSC TEST FAILED

The reference oscillator on the A5 synthesizer does not work properly. This message is displayed when an internal test 6: A5 REFERENCE OSC fails. Troubleshoot the source group in accordance with Chapter 7.

220 FRACTIONAL N OSC TEST FAILED

The fractional N oscillator on the A5 synthesizer does not work properly. This message is displayed when an internal test 7: A5 FRACTIONAL N OSC fails. Troubleshoot the source group in accordance with Chapter 7.

221 STEP OSC TEST FAILED

The step oscillator on the A5 synthesizer does not work properly. This message is displayed when an internal test 8: A5 STEP OSC fails. Troubleshoot the source group in accordance with Chapter 7.

222 1st LO OSC TEST FAILED

The 1st LO OSC (first local oscillator) on the A4A1 1st LO does not work properly. This message is displayed when an internal test 9: A4A1 1ST LO OSC fails. Troubleshoot the source group in accordance with Chapter 7.

223 **2nd LO OSC TEST FAILED**

The 2nd LO OSC (second local oscillator) on the A3A2 2nd LO does not work properly. This message is displayed when an internal test 10: A3A2 2ND LO fails. Troubleshoot the source group in accordance with Chapter 7.

224 **A3 DIVIDER OUTPUT FREQUENCY OUT OF SPEC**

The output frequency of the divider circuit on the A3A1 ALC is out of its limits. This message is displayed when an internal test 11: A3A1 DIVIDER fails. Troubleshoot the source group in accordance with Chapter 7.

225 **3rd LO OSC TEST FAILED**

The 3rd LO OSC (third local oscillator) on the A6 receiver IF does not work properly. This message is displayed when an internal test 12: A6 3RD LO OSC fails. Troubleshoot the receiver group in accordance with Chapter 8.

226 **SOURCE OSC TEST FAILED**

The source oscillator on the A3A1 ALC does not work properly. This message is displayed when an internal test 13: A3A1 SOURCE OSC fails. Troubleshoot the source group in accordance with Chapter 7.

227 **SAMPLE FREQUENCY OUT OF SPEC**

The sampling frequency of the sample/hold circuit on the A6 receiver IF is out of its limits. This message is displayed when an internal test 15: A6 SEQUENCER fails. Troubleshoot the receiver group in accordance with Chapter 8.

228 **SOURCE LEVEL TEST FAILED**

The source level output from the A3A3 source is out of limits. This message is displayed when an "internal test 15: SOURCE LEVEL" fails. Troubleshoot the source group in accordance with Chapter 7.

229 **DC BIAS TEST FAILED**

The DC bias level is out of limits. This message is displayed when an "internal test 16: DC BIAS" fails. Troubleshoot the source group in accordance with Chapter 7.

230 **FLOPPY DISK DRIVE FAILURE FOUND**

The A53 built-in FDD (floppy disk drive) does not work properly. This message is displayed when an external test 18: DSK DR FAULT ISOL'N fails. Replace the A53 FDD with a new one. See Chapter 6 .

231 **POWER SWEEP LINEARITY OUT OF SPEC**

This message is displayed when an external test 19: POWER SWEEP LINEARITY fails. Troubleshoot the analyzer in accordance with Chapter 4.

232 **SOURCE FLATNESS TEST FAILED**

An "external test 20: SOURCE FLATNESS" fails. Troubleshoot the source group in accordance with Chapter 7.

233 **OUTPUT ATTENUATOR TEST FAILED**

An “external test 21: OUTPUT ATTENUATOR” fails. Troubleshoot the A7 output attenuator in accordance with Chapter 7.

234 **TRD LOSS TEST FAILED**

An “external test 22: TRD LOSS” fails. Troubleshoot transducer group in accordance with Chapter 9 .

235 **TRD ISOL'N I TO V TEST FAILED**

An “external test 28: TRD ISOL'N I TO V” fails. Troubleshoot the transducer group in accordance with Chapter 7.

236 **TRD ISOL'N V TO I TEST FAILED**

An “external test 29: TRD ISOL'N V TO I” fails. Troubleshoot the transducer group in accordance with Chapter 9 .

237 **HI Z HEAD TEST FAILED**

An “external test 30: HIGH Z HEAD” fails. Replace the high impedance test head. See Chapter 9 .

238 **LO Z HEAD TEST FAILED**

An “external test 31: LOW Z HEAD” fails. Replace the low impedance test head. See Chapter 9 .

239 **FRONT ISOL'N TEST FAILED**

An “external test 25: FRONT ISOL'N” fails. Troubleshoot the receiver group in accordance with Chapter 8.

240 **CABLE ISOL'N TEST FAILED**

An “external test 27: ” fails. Troubleshoot the transducer group in accordance with Chapter 9 .

241 **RECEIVER GAIN TEST FAILED**

An “external test 22: RECEIVER GAIN” fails. Troubleshoot the receiver group in accordance with Chapter 8.

242 **RECEIVER GAIN OUT OF SPEC**

An “external test 25: FRONT ISOL'N” fails. A6 receiver IF gain is incorrect. Troubleshoot the receiver group in accordance with Chapter 8.

243 **A6 GAIN TEST FAILED**

An “external test 23: A6 GAIN” fails. Replace the A6 receiver IF. See Chapter 8.

244 **A6 VI NORMALIZER TEST FAILED**

An “external test 24: A6 VI NORMALIZER” fails. Replace the A6 receiver IF. See Chapter 8.

245 **MAX VCXO LEVEL OUT OF SPEC**

Maximum VCXO level is incorrect, in performing an "adjustment test 36: 3RD VCXO LEVEL ADJ" or an "adjustment test 39: SOURCE VCXO LEVEL ADJ". In the 3RD VCXO LEVEL ADJ, replace the A6 receiver IF. In the SOURCE VCXO LEVEL ADJ, replace the A3A1 source vernier.

246 **VCXO TUNING VOLTAGE OUT OF LIMIT**

VCXO tuning voltage is incorrect, in performing an "adjustment test 36: 3RD VCXO LEVEL ADJ" or an "adjustment test 39: SOURCE VCXO LEVEL ADJ". In the 3RD VCXO LEVEL ADJ, replace the A6 receiver IF. In the SOURCE VCXO LEVEL ADJ, replace the A3A1 source vernier.